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Original Research Article

Study and simulation of scalable demultiplexer hardware by using different VHDL modeling for communication system

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ABSTRACT
The paper provides a general overview of demultiplexers chips as well as their applications. The multiplexers and demultiplexers play an important part in the designing of Communication systems. Both have different work multiplexer combines different signals and through them over a signal channel. Whereas demultiplexer gives a single channel signal to multiple lines which depends upon the value of selection lines. In this paper, the chip design is done for(1×16) demux, (1×32) demux, and (1×64) demux in VHDL with various types of VHDL modeling like data flow, behavioral and structural modeling, and also their simulation to see its waveforms in ISE design suite 14.7. Demultiplexer design helps the designers estimate the chip performance and timing, memory, and hardware utilization parameters. The comparison is done for these three types of modeling on the FPGA Virtex-5 based on the number of slices used, LUT used, total combinational path delay, and the memory utilized by the design. So it will help the researcher to know which type of modeling is better for the designing of demux (1×16), demux (1×32), and demux (1×64).The results show that for (1×64) demux in data flow modeling the delay is the largest and also the memory utilization is the largest compared to that of (1×16) demux, and (1×64) demux. In behavioral modeling, the delay is equal for all three demux that is (1×16) demux, (1×32) demux, and (1×64) demux, and memory utilization is largest for (1×64) demux. whereas in the case of structural modeling, the delay and slices used are larger for demux (1×32), and I/Os and memory utilization are greatest for demux (1×64).

1. Introduction

The data distributor is exactly the reverse of the multiplexer we studied earlier and is more commonlyreferredto as a demultiplexer or "Demux" for short instruction. The demultiplexer switches a unique input data line to each of several separate output lines, one at a time. Demultiplexers produce several outputs from unique data inputs and several selection inputs. Depending on the values of the input selection line, it permits the data supplied to one of the outputs. Demultiplexers can be useful when designing general-purpose logic because they can function as a decoder if their input is always true. Demultiplexer, often known as DEMUX, is a digital device that can forward its unique input onto any of the several output lines. The single input and numerous outputs of a demultiplexer. It has 2^n output lines where "n" represents the number of control signals. Every control signal combination chooses a particular output line through which the input data signal should exit. Output lines are also known by the name channels. The way a demultiplexer works is exactly the opposite of a multiplexer.

All of the phone (and data) lines on a customer's phone line in telephony have been bundled together, using a multiplexer and the only way to access them is through a demultiplexer. Even though the connections are often not encrypted, this allows for more secure communications where such demultiplexers are rare. The Chemical etching of silicon substrates to create athlete gratings has already proven to be effective, simple to use, and well-suited for optical wavelength demultiplexing. In this research, experimentalists and theoreticians work together to develop feasible wavelength demultiplexers for optical communications in the ranges of 0.78–0.9 and 1.2-1.35 micrometers [1].A grating demultiplexer coupler is the only device that has the quality of light and demultiplexer. In this paper, all about this is discussed [2]. To extract four different wavelengths near frequencies corresponding to communication windows, the studied demultiplexer is built on optical filters with optimized parameters. The most crucial aspect of communication systems is thought to be optical filtering devices [3]. This article presents a novel photonic crystal fiber-based 1x2 power demultiplexer concept. By introducing flaws in the photonic crystal fiber (PCF) structure as the shift in the silica and air index, the luminary connection between the center core and coherent laser sources is made possible [4]. Critical photonic components known as microring resonators are used in nonlinear, sensing, and filtering applications. The Micro Ring Resonator (MRR) has recently found use in the creation of optical logic gates. This paper discusses the operation of an MRR-based demultiplexer. MRR functions t optical switching apparatus [5].

An appropriate substrate can be drilled with holes to create a two-dimensional photonic crystal using photolithography. This research suggests and simulates an 8-channel demultiplexer built on 2D photonic crystals for WDM and DWDM applications. The best quality factors to date, according to the literature, were attained [6].

A 116 GS/s analog demultiplexer front-end is shown in this work, sampling one differential input channel and cycling it to four differential outputs at 29 GS/s each [7]. This study describes a two-channel wavelength division demultiplexer that divides 1532.68 and 1596.34 nm wavelengths into separate ports with a loss of about 3 dB. The device is based on a multimode interferometer [8]. The research presented here suggests a Photonic Crystal (PhC) structure based on a 3×1 Multiplexer/ Demultiplexer (MUX/DEMUX) [9]. One input line and two output lines (i.e., two transmission channels) make up this demultiplexer. In demux (1×2) one input line and two output channels are attached at the same place. The length of each waveguide of the proposed structure's asymmetric loops is particularly sensitive to the Fano resonances, which are produced by this system. [10].

All optical demultiplexing constructed on photonic crystals is presented and simulated in this study for a communication system. This work silicon substrate and a thin coating of silica with a specified 2-dimensional rectangular pattern of holes as a photonic crystal [11]. It is suggested and proved to use a two-dimensional square lattice photonic crystal (PC)-based silicon rod-based all-optical 1×2 De-multiplexer (Demux). Phase differences between input beams caused by point defects and line and point flaws are what cause the device to operate [12]. Spatial mode demultiplexing is offered by Volume holographic demultiplexers (VHDMs) employing straightforward optical technologies. In this study, they suggest a dual-wavelength technique (DWM) in conjunction with a VHDL system mode demultiplexing in the optical transmission bands by using the DWM [13]. The planned optical-based tunable OFDM signal demultiplexer is made up of a phase modulator and a tunable chromatic dispersion emulator [14]. There are high transmission losses in visible light communication systems. A unique design was suggested for a 14-optical demultiplexer to address this issue based on multimode interference [15]. The multiplexers and demultiplexes have been used in the network-on-chip operations for ring NoC for selection [16] and processing multiple node data in specific networks. The control memory and data are stored based on this node selection strategy. It has been used for route data communication and directing the data to the specific port for the 2D router [17].

2. Materials and methods

Xilinx ISE 14.7 software is used for designing demux (1×16), demux (1×32), demux (1×64), and Virtex -5 FPGAfor logic verification.

Demux Block Diagram (1×16): Figure 1 shows the block diagram of a (1×16) Demultiplexer using five (1×4) demux. Assuming that D_{in} is the input, the selection lines are S_3 and S_2, S_1, and S_0 . Q_0 to Q_{15} are sixteen outputs. In the logical equations Q_0, Q_1, Q_2, Q_3…….Q_{15} are outputs and S_0, S_1, S_2, S_3 are the selection lines, D_{in} is the input given to (1×16) demux.

$$Q_0 = \bar{s_3}\bar{s_2}\bar{s_1}\bar{s_0}D_{in} \quad (1)$$

$$Q_1 = \bar{s_3}\bar{s_2}\bar{s_1}s_0D_{in} \quad (2)$$

$$Q_2 = \bar{s_3}\bar{s_2}s_1\bar{s_0}D_{in} \quad (3)$$

……..

$$Q_{15} = s_3\, s_2 s_1 s_0\, D_{in} \quad (15)$$

and D_{in}=1

Demux Block Diagram (1×32): Figure 2 shows the block diagram of demux (1×32) using demux (1×4), demux (1×8), and demux(1×4) has two selections lines s_0,s_1, and demux (1×8) has three selection line s_2 ,s_3, s_4. Total selection line for (1×32) Demuxis five in number which are s_0, s_1 s_2 ,s_3, s_4, and the output lines are from Q_0Q_1,Q_2,Q_3, to……Q_{31}. And D_{in} is the input that is given to the demultiplexer.
Logical equations $Q_0, Q_1, Q_2, Q_3, Q_4, Q_5$to…… $Q_{31}$are given as follows.

$$Q_0 = \bar{s_4}\bar{s_3}\bar{s_2}\bar{s_1}\bar{s_0}D_{in} \quad (16)$$

$$Q_1 = \bar{s_4}\bar{s_3}\bar{s_2}\bar{s_1}s_0D_{in} \quad (17)$$

$$Q_2 = \bar{s_4}\bar{s_3}\bar{s_2}s_1\bar{s_0}D_{in}, \quad (18)$$

$$Q_3 = \bar{s_4}\bar{s_3}\bar{s_2}s_1s_0D_{in} \quad (19)$$

$$Q_4 = \bar{s_4}\bar{s_3}s_2\bar{s_1}\bar{s_0}D_{in}, \quad (20)$$

$$Q_6 = \bar{s_4}\bar{s_3}s_2\bar{s_1}s_0D_{in} \quad (21)$$

……

$$Q_{31} = s_4s_3s_2s_1s_0D_{in} \quad (47)$$

Demux Block Diagram (1×64): Figure 3 shows the block diagram of (1×64) demuxusing (1×4) demux and (1×16) demux. Demux (1×4) has two selection line s_0, s_1,and demux (1×16) has four selections lines s_2, s_3,s_4, s_5 . The total number of selection line for demux (1×64) are six in number which are s_0, s_1, s_2, s_3,s_4, s_5 and the output lines are from Q_0, Q_1, Q_2, Q_3, Q_4……Q_{63}. And D_{in} is the input that is given as input to the demux (1×64).
The logical equations $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6$ to……. $Q_{63}$are given as follows.

$$Q_0 = \bar{s_5}\bar{s_4}\bar{s_3}\bar{s_2}\bar{s_1}\bar{s_0}D_{in} \quad (48)$$

$$Q_1 = \bar{s_5}\bar{s_4}\bar{s_3}\bar{s_2}\bar{s_1}s_0D_{in} \quad (49)$$

$$Q_2 = \bar{s_5}\bar{s_4}\bar{s_3}\bar{s_2}s_1\bar{s_0}D_{in} \quad (50)$$

$$Q_3 = \bar{s_5}\bar{s_4}\bar{s_3}\bar{s_2}s_1s_0D_{in} \quad (51)$$

$$Q_4 = \overline{s_5}\,\overline{s_4}\,\overline{s_3}\,s_2\,\overline{s_1}\,\overline{s_0}\,D_{in} \quad (52)$$

$$Q_5 = \overline{s_5}\,\overline{s_4}\,\overline{s_3}\,s_2\,\overline{s_1}\,s_0\,D_{in}\ , \quad (53)$$

……

$$Q_{63} = s_5 s_4 s_3 s_2 s_1 s_0 D_{in} \quad (110)$$

The demultiplexer design will help the designers or the researchers estimate the chip performance and delay, memory used, and hardware utilization parameters in the various types of VHDL modeling. So we have done a Comparison of these three types of modeling on the FPGA Virtex-5 based on the Number of Slices used, LUT used, Total combinational path delay, and the memory utilized by it. So it will help the researcher to know which type of modeling is better for the designing of demux(1×16), demux (1×32), and demux (1×64).

3. Results and discussion

3.1 Simulation waveforms with different types of modeling

The simulation is carried out on the Xilinx ISE design suite 14.7 in the various types of VHDL modeling such as data flow modeling, behavioral modeling, and structural modeling for demux (1×16), demux (1×32), and demux (1×64).The simulation results obtained are shown in Figures 4, 5 and 6 respectively. Results are depicted in Table 1, also analyzed on FPGA devices like Virtex-5, for different types of modeling in VHDL.

Table 1: Truth table of (1×16) demultiplexer.

D_{in}	S_3	S_2	S_1	S_0	Q_{15}	Q_{14}	Q_{13}	Q_{12}	Q_{11}	Q_{10}	Q_9	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

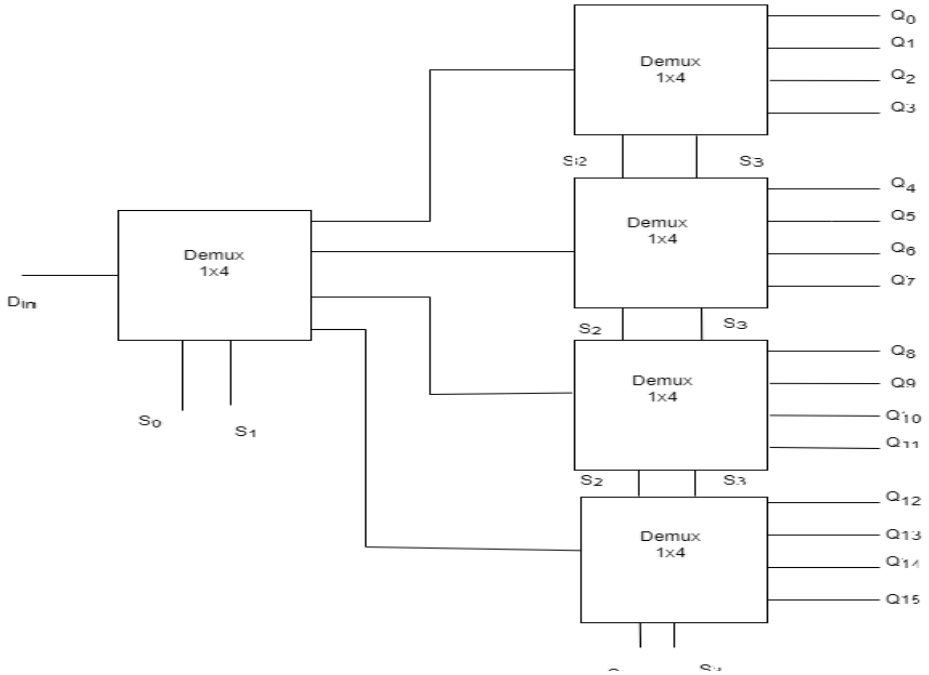

Figure 1: Block representation of 1×16 DEMUX

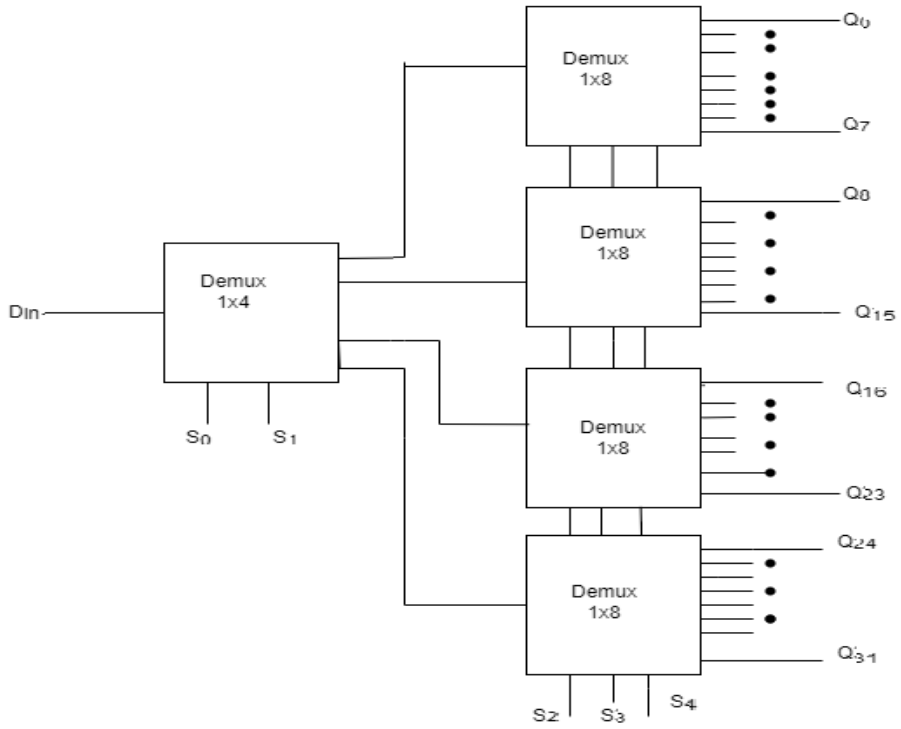

Figure 2: Block representation of demux (1×32).

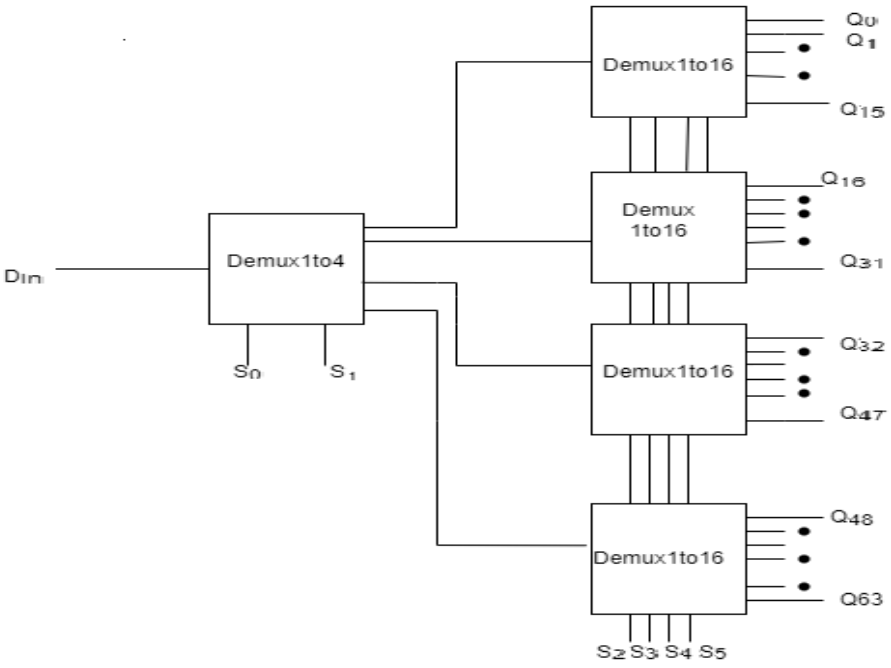

Figure 3: Block representation of (1×64) DEMUX.

3.2 Result analysis

The simulation is carried out on the Xilinx ISE design suite 14.7 in the various types of VHDL modeling, data flow, and behavioral modeling. The modeling for demux (1×16), demux (1×32), and demux (1×64) are done successfully, and also analyzed on devices like Virtex-5, for different types of modeling in VHDL. The software estimated the number of slices used, flip-flops, the number of LUT used, the total input/output of the circuits, and memory used, and also calculated the total delay of the circuit for the individual demux. Results are depicted in Table 4. This helps the researchers to know which type of modeling uses fewer resources and less delay. Through this, we came to know the best modeling for the designing of any demultiplexer chip.

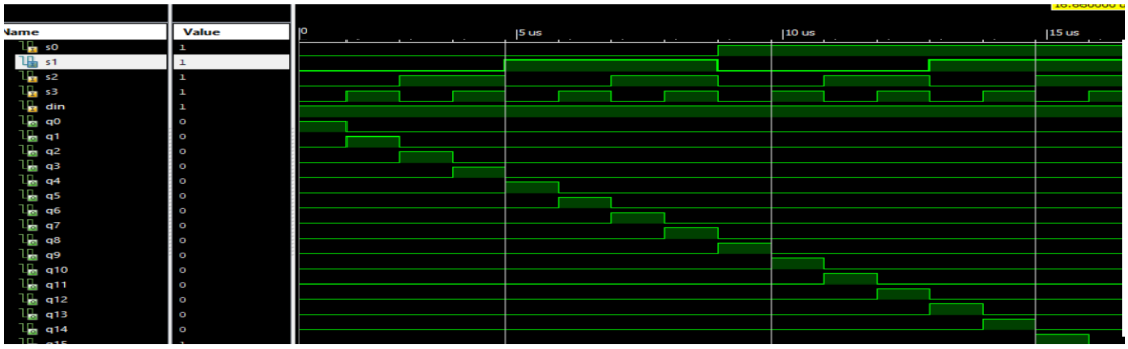

Figure 4: Simulations waveforms for Demux 1×16.

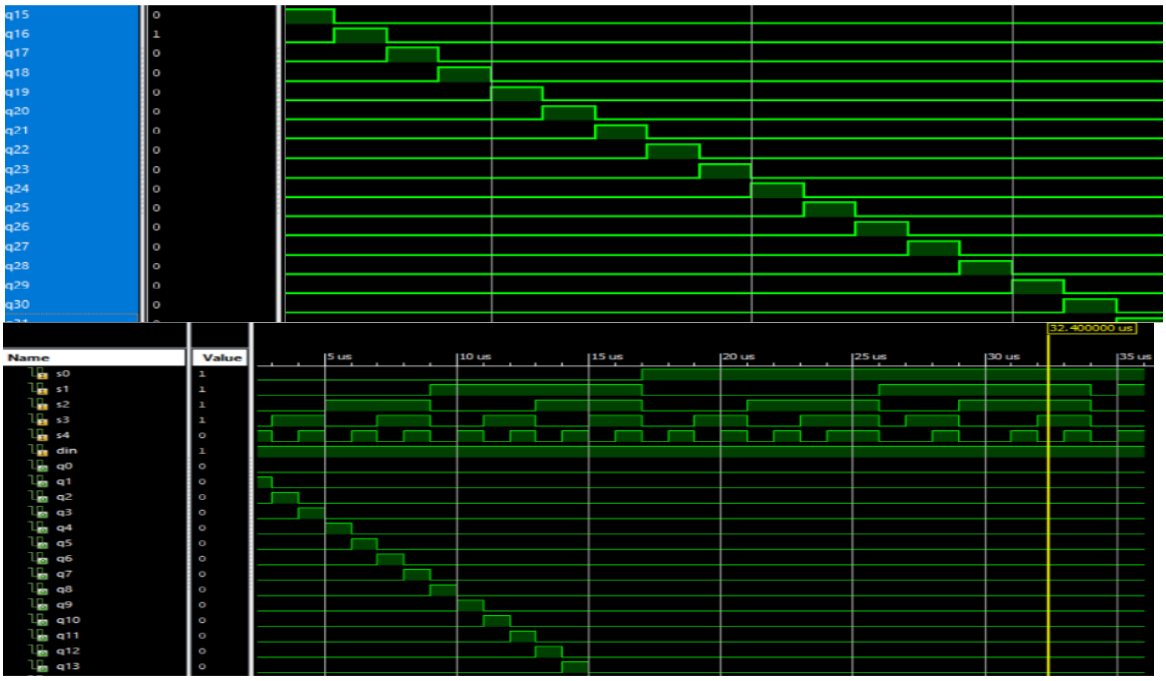

Figure 5: Simulations waveforms for Demux-1×32.

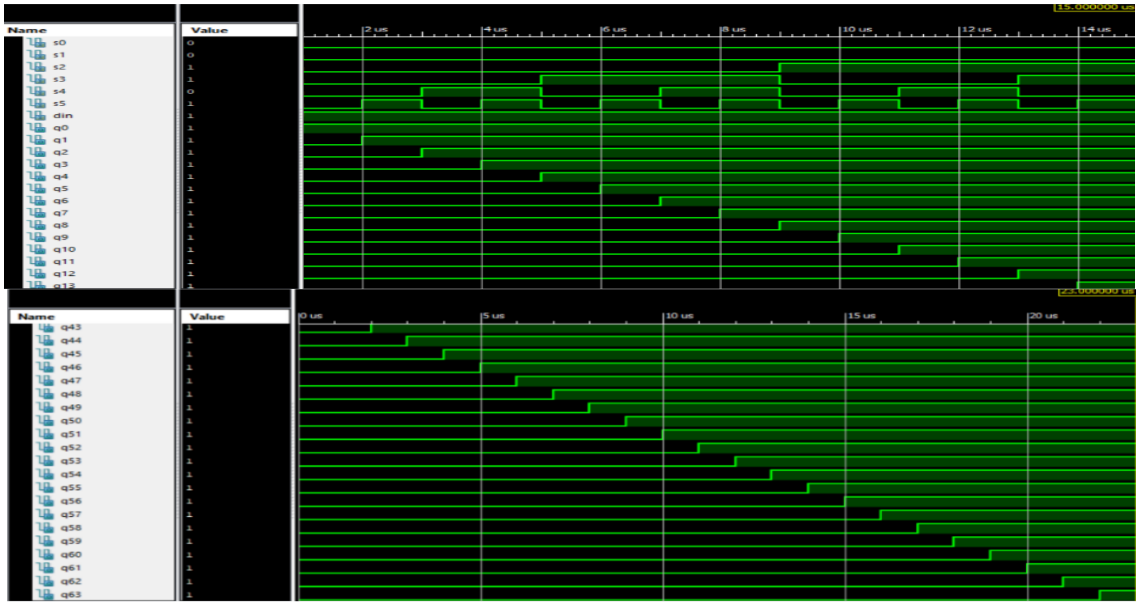

Figure 6: Simulations waveforms for Demux (1×64).

Table 1: Result analysis of different types of modeling.

Modelling &demux / used parameters	Structural Modelling (Demux)			Data Flow modeling (Demux)			Behavioral Modelling (Demux)		
	(1×16)	(1×32)	(1×64)	(1×16)	(1×32)	(1×64)	(1×16)	(1×32)	(1×64)
1.Slices (out of 12480)	16	32	66	32	2	109	16	32	24
2. LUTs (out of 12480)	8	32	66	32	40	109	16	32	24
3. I/Os (out of 172)	21	38	71	21	38	71	21	38	70
4. Delay(ns)	4.098	4.218	4.838	3.040	3.040	3.040	4.098	4.218	4.214
5. Memory (KB)	45499-72	45513-16	45529-16	45296-52	45325-32	45459-82	45285-64	45286-92	45288-20

4. Conclusions

The chip design and simulation are done successfully for demux (1×32), and demux (1×64) with the help of data flow modeling, behavioral modeling, and structural modeling in VHDL. The performance is analyzed by the various parameters used like number of slices used, LUT used, I/Os, delay, and memory u. In the case of data flow modeling the delay is largest for demux (1×64) whereas, in the case of behavioral modeling, the delay for demux (1×16), demux (1×32), and demux (1×64) are equal to 3.040ns. whereas memory utilization in the case of data flow modeling is largest for demux (1×64) which is equal to 4552916KB. Whereas in the case of behavioral modeling, the memory utilization is largest in demux (1×64) which is equal to 45459082KB. In structural modeling, the delay is largest for demux (1×32) which is equal to 4.218 ns and memory utilization is maximum for demux (1×64) which is equal to 4528820KB.

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