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Original Research Article

Study and simulation of scalable multiplexer hardware for communication networks

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ABSTRACT
Multiplexing as a technique provided in a network is used to combine several input signals into a composite signal before it is sent over a shared medium. Multiplexed networks utilize diverse approaches of multiplexing, but conceptually all of them work similarly. A multiplexer (MUX) generates a compound signal by combining the different network signals before transmitting it over a shared channel. The hardware chip design depends on the configuration of the multiplexer in the communication network. The study of this work is conferred as the digital logic design and simulation of various configurations of the multiplexer hardware. The evaluation of performance is also measured on the Virtex-5 series of Xilinx FPGA and the functionality of each configured design is checked logically on ISE 14.7 software. The simulation and current analysis of the chip design of various configurations of multiplexer assists the designers to check the chip performance, memory, timing, and hardware implementation parameters which can be further incorporated with specific networks.

1. Introduction

The development of multiplexer technologies has accompanied that of digital communication, networking, and computing in recent years. Multiplex networks [1, 2] which feature several levels of different interconnections amid constituents as well as the interaction between these interconnection layers, are used by many complex real-world systems to carry out their emergent functions. To simulate the characteristics of integrated social networks, multiplex networks are used. The interconnections in several composite systems including society, transportation, biology, etc. have been effectively defined using network theory [3-5]. Multiple connection channels are used in systems known as multi-layer networks. Each channel is made up of layers, and nodes in various levels often have various kinds of connections. The multiplex network is the name given to such a complicated model [6].

A crucial component of multiplex dynamic networks is synchronization. Additionally, the issue of network synchronization has gained a lot of attention in the area of brain signals [7]. Currently, the challenge of synchronizing the layers of multilayer networks and diverse networks interacting with one another arose in conjunction with the development of concepts about complex networks [8]. The global and local connection requirements for achieving definite and steady-time phase-frequency order are met by using a unique multiplex control [9].

In the Internet of Things (IoTs), at the time of communication multiplex networks may efficiently constitute network data produced by the sensors integrated across many platforms [10]. One of the most significant advancements in Fourier ptychographic microscopy (FPM) that significantly speeds up picture acquisition and reconstruction is the multiplex lighting system used in the Internet of Medical Things (IoMT).On multiplex networks the interactions between illness and disease-based information were examined [11, 12].

The challenges to energy security throughout the switch to renewable energy systems move from crude oil to vital minerals like cobalt. Thus, in the next age of renewable energy, comprehending the global cobalt industrial chain has become a new difficulty. Network scientists see the worldwide cobalt industrial chain as a multiplex network [13]. Internet of things, high-definition video streaming, online gaming, and other low latency and high bandwidth network applications have become more common in recent years. To combine various audio or video signals into a single transmission stream for audio and video broadcasting systems, multiplexers are used [14].

The fundamental characteristics of WDM are consistent spectral division and modulation levels, which restrict flexibility and resource application in these networks. As a result, it has been suggested that the primary characteristic of elastic optical networks is the usage of the radio spectrum of optical fibers in the absence of permanent and preset partition [15, 16].

The proposed study considers the multi-input information approach in designing various configurations of multiplexers. The various multiplexer configurations determine the timing, memory, and hardware utilization parameters in terms of slices, look-up tables (LUTs), memory consumption, combinational delay, etc.

The contributions of this study are many folds as awareness about the advantages of multiplexed networks, to

know the different indices of field programmable gate array (FPGA) used to check the performance evaluation of the same digital logic by using timing and hardware utilization.

(a)

Inputs	Output
$S_0 S_1 S_2 S_3$	Y
0 0 0 0	X_0
0 0 0 1	X_1
0 0 1 0	X_2
0 0 1 1	X_3
0 1 0 0	X_4
0 1 0 1	X_5
0 1 1 0	X_6
0 1 1 1	X_7
1 0 0 0	X_8
1 0 0 1	X_9
1 0 1 0	X_{10}
1 0 1 1	X_{11}
1 1 0 0	X_{12}
1 1 0 1	X_{13}
1 1 1 0	X_{14}
1 1 1 1	X_{15}

(b)

Inputs	Output
$S_0 S_1 S_2 S_3 S_4$	Y
0 0 0 0 0	X_0
0 0 0 0 1	X_1
0 0 0 1 0	X_2
0 0 0 1 1	X_3
0 0 1 0 0	X_4
0 0 1 0 1	X_5
0 0 1 1 0	X_6
0 0 1 1 1	X_7
0 1 0 0 0	X_8
0 1 0 0 1	X_9
0 1 0 1 0	X_{10}
: : : : :	:
: : : : :	:
1 1 1 0	X_{30}
1 1 1 1	X_{31}

(c)

Inputs	Output
$S_0 S_1 S_2 S_3 S_4 S_5$	Y
0 0 0 0 0 0	X_0
0 0 0 0 0 1	X_1
0 0 0 0 1 0	X_2
0 0 0 0 1 1	X_3
0 0 0 1 0 0	X_4
0 0 0 1 0 1	X_5
0 0 0 1 1 0	X_6
0 0 0 1 1 1	X_7
0 0 1 0 0 0	X_8
0 0 1 0 0 1	X_9
0 0 1 0 1 0	X_{10}
: : : : : :	:
: : : : : :	:
1 1 1 1 0	X_{62}
1 1 1 1 1	X_{63}

Figure 1: Functional table of (a) (16×1) MUX, (b) (32×1) MUX, (c) (64×1) MUX.

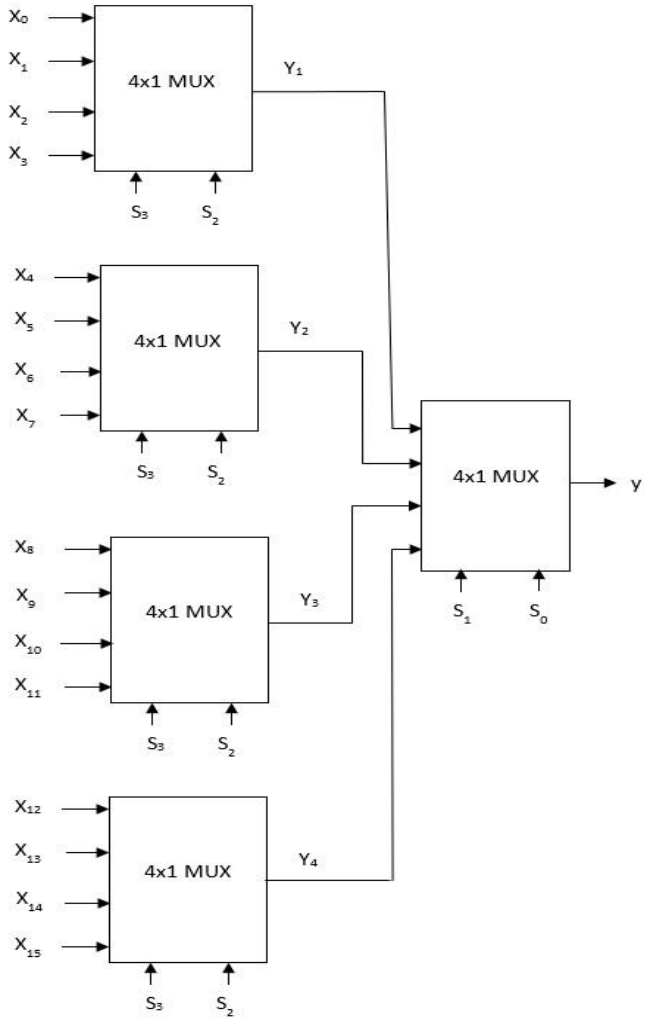

Figure 2: (16×1) MUX by using (4×1) MUXs

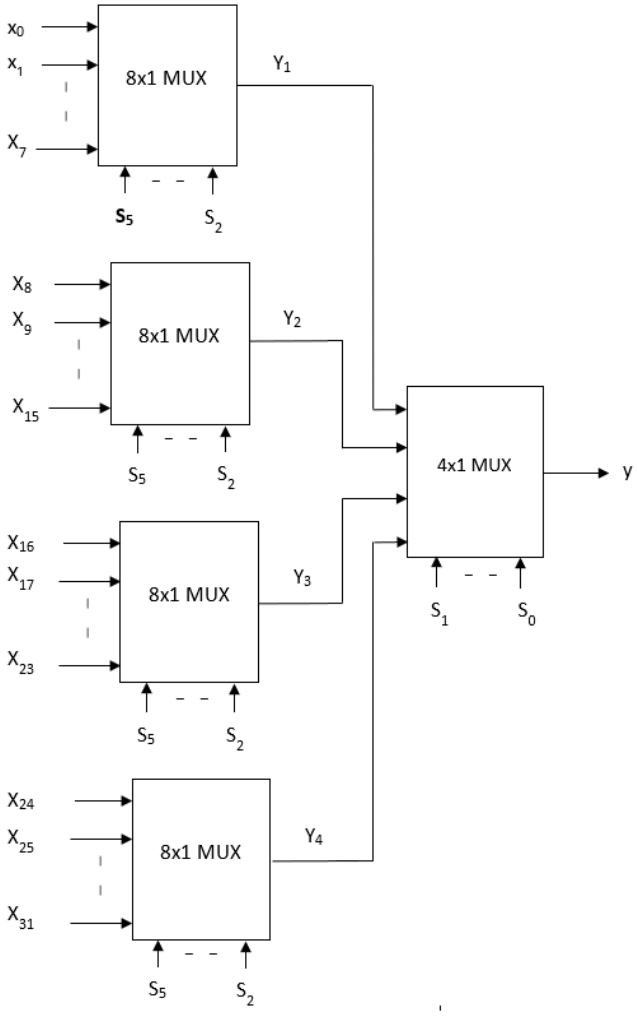

Figure 3: (32×1) MUX by using (8×1) and (4×1) MUXs.

2. Materials and methods

2.1 Materials

The chip design is done with the help of Xilinx ISE 14.7 software and Virtex-5 series of Xilinx FPGA hardware kit is utilized for the synthesis of the designed chip.

2.2 Methods

The following technique is provided to assist the design. The process involves chip analysis and step-by-step execution like Constraints on design, design approach, modeling approach, RTL analysis, functional simulation, Test cases analysis, FPGA synthesis, parameters analysis, and at last comparative analysis are the typical phases.

Design Constraints: Select the size of multiplexer as the clustered data. For example, the design is based on like (16×1), (32×1) and (64×1) configurations of MUX.

Design Approach: The (16×1) multiplexer is a network device that contains four selection lines (S_0 to S_3) and sixteen numbers of input choices (X_0 to X_{15}). It has single output, Y, which, is linked to one of the sixteen choices of input depending on the signals received by selection lines (S_0 to S_3).

Similarly, (32×1) and (64×1) multiplexers contain five (S_0 to S_4) and six (S_0 to S_5) selection lines, thirty-two (X_0 to X_{31}) and sixty-four (X_0 to X_{63}) numbers of input choices respectively. They also have a single output, Y, which is linked to one of the input lines according to the signals received by the selection lines.

The functional table of (16×1), (32×1), and (64×1) MUXs is presented in Figure 1 and the design of (16×1), (32×1), and (64×1) MUXs are depicted in Figures 2, 3 and 4 respectively in the form of block diagram representation. The design of the MUXs is based on modular approach in which each configuration of MUXs is implemented by dividing the whole configuration into five modules like the design of (16×1) MUX has five (4×1) MUXs, design of (32×1) MUX has four (8×1) MUXs and one (4×1) MUX similarly (64×1) MUX has four (16×1) MUXs and one (4×1) MUX.

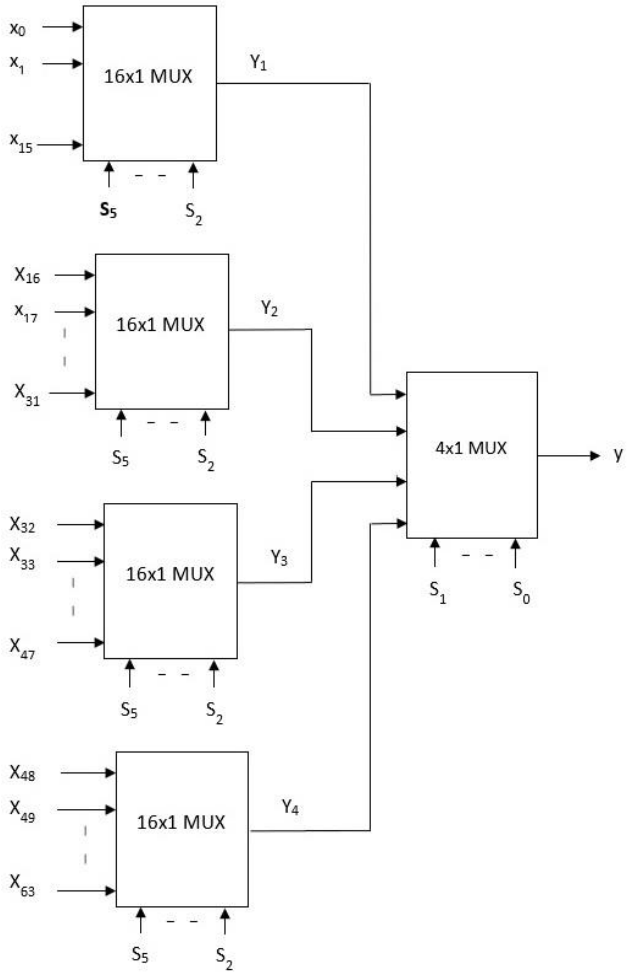

Figure 4: (64×1) MUX by using (16×1) and (4×1) MUXs.

The output Y of (16×1), (32×1), and (64×1) MUXs in logical form are given by Eqs. (1), (2) and (3) respectively.

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2\,\bar{S}_3X_0 + \bar{S}_0\bar{S}_1\bar{S}_2\,S_3X_1 + \bar{S}_0\,\bar{S}_1S_2\bar{S}_3X_2 + \bar{S}_0\bar{S}_1S_2S_3X_3 + \bar{S}_0S_1\bar{S}_2\bar{S}_3X_4 + \bar{S}_0S_1\bar{S}_2S_3X_5 + \bar{S}_0S_1S_2\bar{S}_3X_6 + \bar{S}_0S_1S_2S_3X_7 + S_0\bar{S}_1\bar{S}_2\,\bar{S}_3X_8 + S_0\bar{S}_1\bar{S}_2S_3X_9 + S_0\bar{S}_1S_2\bar{S}_3X_{10} + S_0\bar{S}_1S_2S_3X_{11} + S_0S_1\bar{S}_2\bar{S}_3\,X_{12} + S_0S_1\bar{S}_2S_3X_{13} + S_0S_1S_2\bar{S}_3X_{14} + S_0S_1S_2S_3X_{15} \quad (1)$$

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4X_0 + \bar{S}_0\bar{S}_1\bar{S}_2\bar{S}_3S_4X_1 + \bar{S}_0\bar{S}_1\bar{S}_2S_3\bar{S}_4X_2 + \bar{S}_0\,\bar{S}_1\bar{S}_2S_3S_4X_3 + \bar{S}_0\bar{S}_1S_2\bar{S}_3\bar{S}_4X_4 + \bar{S}_0\bar{S}_1S_2\bar{S}_3S_4X_5 + \bar{S}_0\bar{S}_1S_2S_3\bar{S}_4X_6 + \bar{S}_0\bar{S}_1S_2S_3S_4X_7 + \bar{S}_0S_1\bar{S}_2\bar{S}_3\bar{S}_4X_8 + \bar{S}_0S_1\bar{S}_2\bar{S}_3S_4X_9 + \bar{S}_0S_1\bar{S}_2S_3\bar{S}_4X_{10} + \bar{S}_0S_1\bar{S}_2\,S_3S_4X_{11} + \bar{S}_0S_1S_2\bar{S}_3\bar{S}_4X_{12} + \bar{S}_0S_1S_2\bar{S}_3S_4X_{13} + \bar{S}_0S_1S_2S_3\bar{S}_4X_{14} + \bar{S}_0S_1S_2S_3S_4X_{15} + S_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4X_{16} + S_0\bar{S}_1\bar{S}_2\bar{S}_3S_4X_{17} + S_0\bar{S}_1\bar{S}_2S_3\bar{S}_4X_{18} + S_0\bar{S}_1\bar{S}_2S_3S_4X_{19} + S_0\bar{S}_1S_2\bar{S}_3\bar{S}_4X_{20} + S_0\bar{S}_1S_2\bar{S}_3S_4X_{21} + S_0\bar{S}_1S_2S_3\bar{S}_4X_{22} + S_0\bar{S}_1S_2S_3S_4X_{23} + S_0S_1\bar{S}_2\bar{S}_3\bar{S}_4X_{24} + S_0S_1\bar{S}_2\bar{S}_3S_4X_{25} + S_0S_1\bar{S}_2S_3\bar{S}_4X_{26} + S_0S_1\bar{S}_2\,S_3S_4X_{27} + S_0S_1S_2\bar{S}_3\bar{S}_4X_{28} + S_0S_1S_2\bar{S}_3S_4X_{29} + S_0S_1S_2S_3\bar{S}_4X_{30} + S_0S_1S_2S_3S_4X_{31} \quad (2)$$

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4\bar{S}_5X_0 + \bar{S}_0\bar{S}_1\bar{S}_2\bar{S}_3\bar{S}_4S_5X_1 + \bar{S}_0\bar{S}_1\bar{S}_2\bar{S}_3S_4\bar{S}_5X_2 + \bar{S}_0\,\bar{S}_1\bar{S}_2\bar{S}_3S_4S_5X_3 + \bar{S}_0\bar{S}_1\bar{S}_2S_3\bar{S}_4\bar{S}_5X_4 + \bar{S}_0\bar{S}_1\bar{S}_2S_3\bar{S}_4S_5X_5 + \bar{S}_0\bar{S}_1\bar{S}_2S_3S_4\bar{S}_5X_6 + \bar{S}_0\bar{S}_1\bar{S}_2S_3S_4S_5X_7 + \bar{S}_0\bar{S}_1S_2\bar{S}_3\bar{S}_4\bar{S}_5X_8 + \bar{S}_0\bar{S}_1S_2\bar{S}_3\bar{S}_4S_5X_9 + \bar{S}_0\bar{S}_1S_2\bar{S}_3S_4\bar{S}_5X_{10} + \bar{S}_0\bar{S}_1S_2\bar{S}_3\,S_4S_5X_{11} + \bar{S}_0\bar{S}_1S_2S_3\bar{S}_4\bar{S}_5X_{12} + \bar{S}_0\bar{S}_1S_2S_3\bar{S}_4S_5X_{13} + \bar{S}_0\bar{S}_1S_2S_3S_4\bar{S}_5X_{14} + \bar{S}_0\bar{S}_1S_2S_3S_4S_5X_{15} + \bar{S}_0S_1\bar{S}_2\bar{S}_3\,\bar{S}_4\bar{S}_5X_{16} + \bar{S}_0S_1\bar{S}_2\bar{S}_3\bar{S}_4S_5X_{17} + \bar{S}_0S_1\bar{S}_2\bar{S}_3S_4\bar{S}_5X_{18} + \bar{S}_0S_1\bar{S}_2\bar{S}_3S_4S_5X_{19} + \bar{S}_0S_1\bar{S}_2S_3\bar{S}_4\bar{S}_5X_{20} + \bar{S}_0S_1\bar{S}_2S_3\bar{S}_4S_5X_{21} + \bar{S}_0S_1\bar{S}_2S_3S_4\bar{S}_5X_{22} + \bar{S}_0S_1\bar{S}_2S_3S_4S_5X_{23} + \bar{S}_0S_1S_2\bar{S}_3\bar{S}_4\bar{S}_5X_{24} + \bar{S}_0S_1S_2\bar{S}_3\bar{S}_4S_5X_{25} + \bar{S}_0S_1S_2\bar{S}_3S_4\bar{S}_5X_{26} + \bar{S}_0S_1S_2\bar{S}_3\,S_4S_5X_{27} + \bar{S}_0S_1S_2S_3\bar{S}_4\bar{S}_5X_{28} + \bar{S}_0S_1S_2S_3\bar{S}_4S_5X_{29} + \bar{S}_0S_1S_2S_3S_4\bar{S}_5X_{30} + \bar{S}_0S_1S_2S_3S_4S_5X_{31} + S_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4\bar{S}_5X_{32} + S_0\bar{S}_1\bar{S}_2\bar{S}_3\bar{S}_4S_5X_{33} + S_0\bar{S}_1\bar{S}_2\bar{S}_3S_4\bar{S}_5X_{34} + S_0\bar{S}_1\bar{S}_2\bar{S}_3S_4S_5X_{35} + S_0\bar{S}_1\bar{S}_2S_3\bar{S}_4\bar{S}_5X_{36} + S_0\bar{S}_1\bar{S}_2S_3\bar{S}_4S_5X_{37} + S_0\bar{S}_1\bar{S}_2S_3S_4\bar{S}_5X_{38} + S_0\bar{S}_1\bar{S}_2S_3S_4S_5X_{39} + S_0\bar{S}_1S_2\bar{S}_3\bar{S}_4\bar{S}_5X_{40} + S_0\bar{S}_1S_2\bar{S}_3\bar{S}_4S_5X_{41} + S_0\bar{S}_1S_2\bar{S}_3S_4\bar{S}_5X_{42} + S_0\bar{S}_1S_2\bar{S}_3\,S_4S_5X_{43} + S_0\bar{S}_1S_2S_3\bar{S}_4\bar{S}_5X_{44} + S_0\bar{S}_1S_2S_3\bar{S}_4S_5X_{45} + S_0\bar{S}_1S_2S_3S_4\bar{S}_5X_{46} + S_0\bar{S}_1S_2S_3S_4S_5X_{47} + S_0S_1\bar{S}_2\bar{S}_3\,\bar{S}_4\bar{S}_5X_{48} + S_0S_1\bar{S}_2\bar{S}_3\bar{S}_4S_5X_{49} + S_0S_1\bar{S}_2\bar{S}_3S_4\bar{S}_5X_{50} + S_0S_1\bar{S}_2\bar{S}_3S_4S_5X_{51} + S_0S_1\bar{S}_2S_3\bar{S}_4\bar{S}_5X_{52} + S_0S_1\bar{S}_2S_3\bar{S}_4S_5X_{53} + S_0S_1\bar{S}_2S_3S_4\bar{S}_5X_{54} + S_0S_1\bar{S}_2S_3S_4S_5X_{55} + S_0S_1S_2\bar{S}_3\bar{S}_4\bar{S}_5X_{56} + S_0S_1S_2\bar{S}_3\bar{S}_4S_5X_{57} + S_0S_1S_2\bar{S}_3S_4\bar{S}_5X_{58} + S_0S_1S_2\bar{S}_3\,S_4S_5X_{59} + S_0S_1S_2S_3\bar{S}_4\bar{S}_5X_{60} + S_0S_1S_2S_3\bar{S}_4S_5X_{61} + S_0S_1S_2S_3S_4\bar{S}_5X_{62} + S_0S_1S_2S_3S_4S_5X_{63} \quad (3)$$

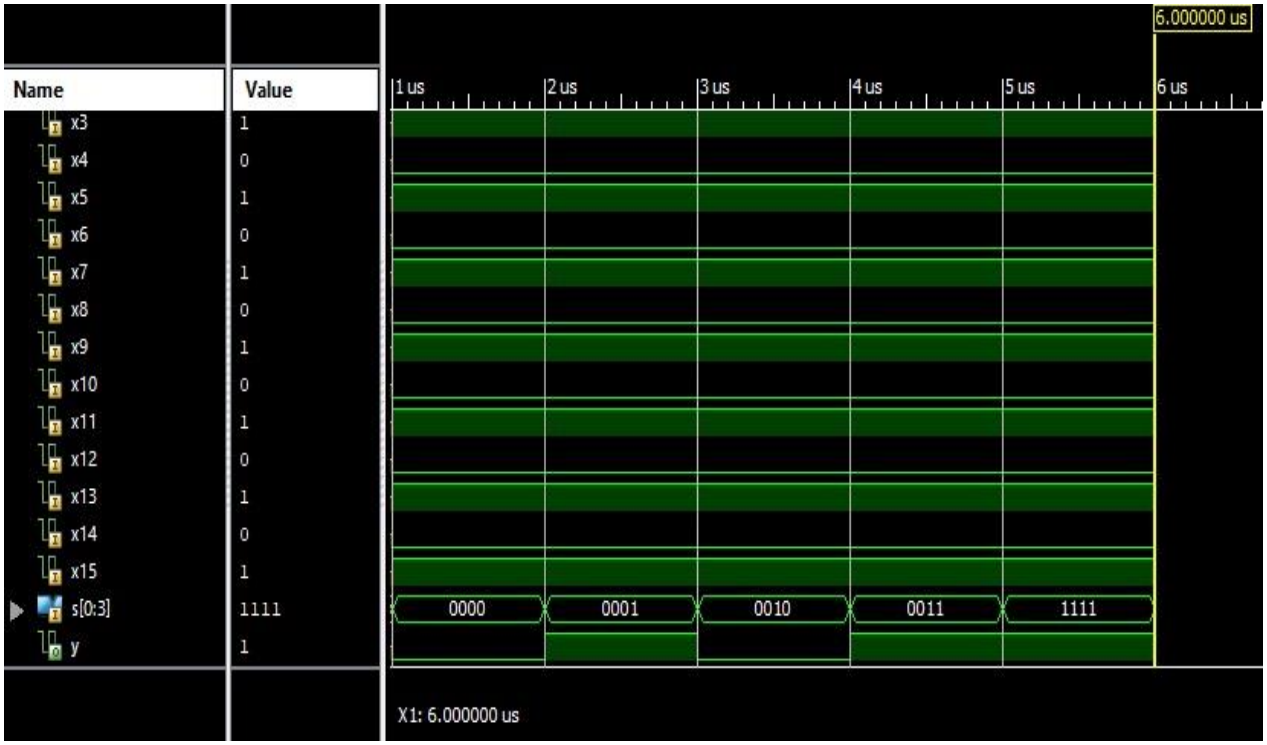

Figure 5: Simulation waveforms of (16×1) MUX.

Figure 6: Simulation waveforms of (32×1) MUX.

Modeling Approach: The design adheres to modelling and design that are based on VHDL. In the ISE 14.7 software, it may have the data-flow model, behavioral model, and structural model.

RTL Analysis: The number of pins that are utilized in the design is shown in the RTL. Based on the input and output direction pins, it is verified.

Functional Simulation: For the functional simulation utilized to evaluate various test cases and inputs for all the developed semiconductors, the Xilinx ISIM waveform simulator is used.

Test Cases Analysis: It is possible to examine the output in waveforms with various time delays and input to output nodes using various test samples and scenarios.

FPGA Synthesis: Locking the pins in the FPGA Kit is followed by logic application insertion, and burning the programme in the FPGA using the Virtex-5 FPGA synthesis approach.

Parameter Analysis: Slices, look-up tables (LUTs), input-output blocks (IoBs), and memory are among the hardware characteristics of the FPGA that are examined. Analysis also requires the timing characteristics, such as delay and frequency.

Comparative Analysis: In order to determine the performance of multiplexer chips with various configuration-based designs in terms of hardware, memory, and timing simulation, comparative analysis is carried out for the hardware and timing parameters.

3. Results and discussion

The simulation of (16×1), (32×1), and (64×1) MUXs is carried out in ISE 14.7 and the result obtained is presented in Figures 5, 6 and 7 respectively.

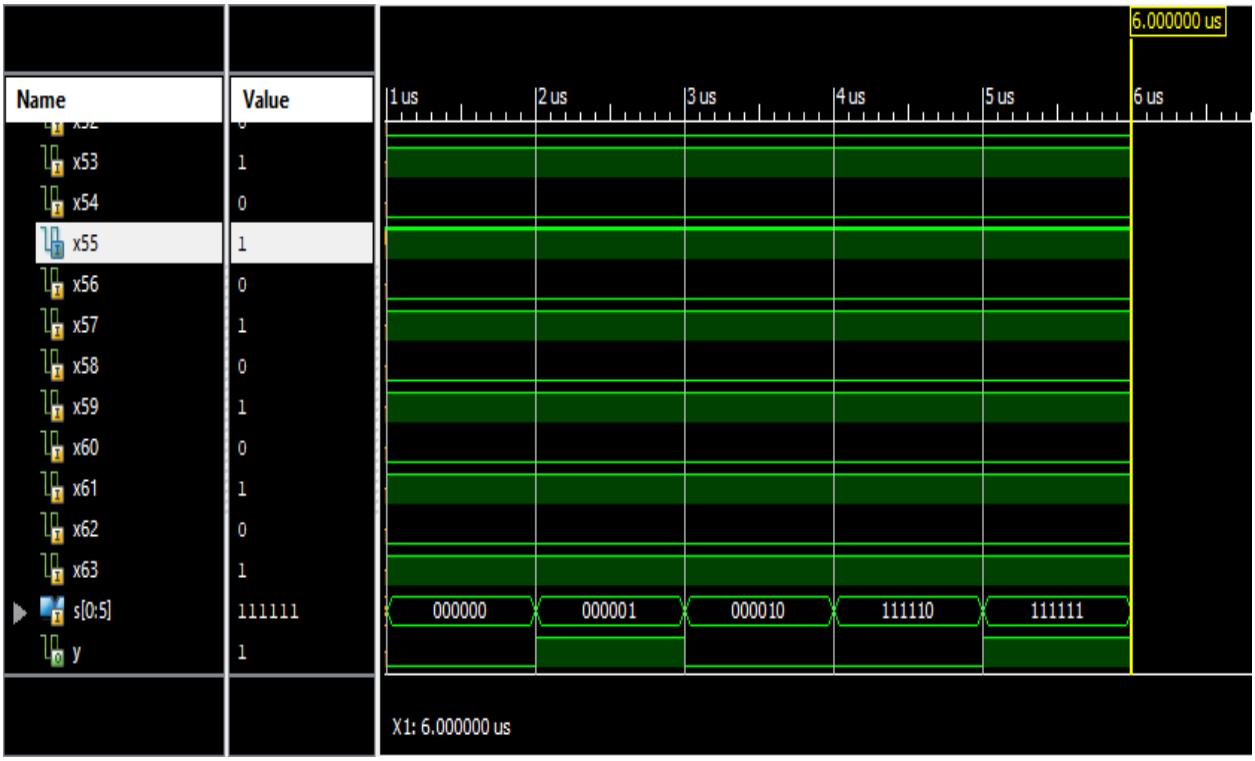

Figure 7: Simulation waveforms of (64×1) MUX.

Table 1: Comparison of different configurations of the multiplexer for various modeling on Virtex-5.

Modeling / FPGA Parameters	Multiplexer (16×1)			Multiplexer (32×1)			Multiplexer (64×1)		
	Data-flow	Behavioral	Structural	Data-flow	Behavioral	Structural	Data-flow	Behavioral	Structural
Slices	4/3120	2/3120	4/3120	4/3120	6/3120	7/3120	18/3120	15/3120	25/3120
LUTs	5/12480	5/12480	5/12480	11/12480	10/12480	8/12480	28/12480	21/ 12480	38/12480
I/Os	20/172	21/172	21/172	38/172	38/172	30/172	71/172	71/172	67/172
Delay (ns)	5.668	5.709	5.668	6.417	6.128	6.253	6.590	6.842	7.591
Memory (kb)	4551876	4550292	4550932	4552020	4549908	4551252	4556116	4550228	4554324

Table 1 shows the result obtained from Virtex-5 FPGA for (16×1), (32×1), and (64×1) configurations of multiplexers. From the table, it is observed that among the data-flow modeling, behavioral modeling and structural modeling the behavioral modeling outperformed in terms of the number of slices, LUTs, and memory consumption.

4. Conclusions

The simulation and hardware chip design are done successfully by using different modeling of VHDL language for various configurations of the multiplexer at Xilinx ISE 14.7. The design concept is based on scalable design and data flow, behavioral and structural modeling's are followed to estimate the performance of the system on the Virtex-5 FPGA hardware kit. The slices used in (64×1) MUX design are 18, 15, and 25 for data flow, behavioral and structural modeling respectively. The LUTs of (64×1) MUX design is 28, 21, and 38 for data-flow, behavioral and structural modeling respectively. The total delay of (64×1) MUX design is 6.590 ns, 6.842 ns, and 7.591 for data flow, behavioral and structural modeling respectively. The memory usage of (64×1) MUX is 4556116 KB, 4550228 KB, and 4554324 KB for data flow, behavioral and structural modeling respectively.

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References

[1] A. Amara, M.A.H. Taieb, M. Ben Aouicha, Cross-network representation learning for anchor users on multiplex heterogeneous social network, *Appl. Soft Comp.* **118** (2022) 108461.

[2] L. Cheng, X. Li, Z. Han, T. Luo, L. Ma, P. Zhu, Path-based multi-sources localization in multiplex networks, *Chaos, Solit. Fract.* **159** (2022) 112139.

[3] D. Fan, B. Sun, H. Dui, J. Zhong, Z. Wang, Y. Ren, Z. Wang, A modified connectivity link addition strategy to improve the resilience of multiplex networks against attacks, *Reliab. Eng. Syst. Safety* **221** (2022) 108294.

[4] Z. Li, J. Tang, C. Zhao, F. Gao, Improved centrality measure based on the adapted PageRank algorithm for urban transportation multiplex networks; *Chaos, Solit. Fract.* **167** (2023) 112998.

[5] R. Lopes, D. Rosário, E. Cerqueira, H. Oliveira, S. Zeadally, Priority-aware traffic routing and resource allocation mechanism for space-division multiplexing elastic optical networks, *Comp. Net.* **218** (2022) 109389.

[6] A. Mahmoudi, A.G. Rahbar, M. Jafari-Beyrami, QoS-Aware routing, space, and spectrum assignment in space division multiplexing networks, *Comp. Net.* **208** (2022) 108920.

[7] E.V. Rybalova, T.E. Vadivasova, G.I. Strelkova, A. Zakharova, Multiplexing noise induces synchronization in multilayer networks, *Chaos, Solit. Fract.* **163** (2022) 112521.

[8] Z. Shao, L. Ma, Q. Lin, J. Li, M. Gong, A.K. Nandi, PMCDM: Privacy-preserving multiresolution community detection in multiplex networks, *Knowledge-Based Syst.* **244** (2022) 108542.

[9] Q. Shi, X. Sun, M. Xu, M. Wang, The multiplex network structure of global cobalt industry chain, *Res. Pol.* **76** (2022) 102555.

[10] F. Tan, L. Zhou, J. Lu, H. Quan, K. Liu, Adaptive quantitative control for finite time synchronization among multiplex switched nonlinear coupling complex networks, *Eur. J. Cont.* **70** (2023) 100764.

[11] J. Wu, X. Li, Finite-time and fixed-time synchronization of Kuramoto-oscillator network with multiplex control, *IEEE Trans. Cont. Net. Syst.* **6** (2018) 863–873.

[12] Q. Wu, S. Chen, Coupled simultaneous evolution of disease and information on multiplex networks, *Chaos, Solit. Fract.* **159** (2022) 112119.

[13] H. Zhang, X. Chen, Y. Peng, G. Kou, R. Wang, The interaction of multiple information on multiplex social networks, *Info. Sci.* **605** (2022) 366–380.

[14] J. Zhang, T. Xu, Y. Zhang, Y. Chen, S. Wang, X. Wang, Multiplex Fourier ptychographic reconstruction with model-based neural network for Internet of Things, *Ad Hoc Net.* **111** (2021) 102350.

[15] S. Zhang, K.L. Yeung, Location constrained virtual optical network embedding in space-division multiplexing elastic optical networks, *Comp. Net.* **220** (2023) 109475.

[16] H. Zhu, X. Yan, Z. Jin, Knowledge transmission model in the multiplex networks with consideration of online and offline channels, *Commun. Nonlin. Sci. Num. Simul.* **108** (2022) 106186.