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Original Research Article

Cadence Virtuoso based circuit simulation of universal logic gates: A board tutorial

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ABSTRACT
Gate-level designs and circuit simulations are fundamental processes for building complex digital circuits. This paper focuses on the design and circuit simulation of two universal digital logic gates viz. NAND and NOR gates using Cadence Virtuoso software. The study leverages the versatile ADE L environment for transient analysis performed on each logic gate to simulate the output response to an input pulse signal. The results of the simulations were plotted as transient graphs to visualize the gate operation properly. The simulated results showed that both NAND and NOR gates were properly operated, which was further validated via their Truth tables. The NAND gate produced only a low output signal, when both of the input signals were high. The NOR gate produced an output signal that was high only, when all of the input signals were low. Through rigorous simulation and meticulous analysis, this research uncovers the dynamic behavior of these logic gates, shedding light on their functionality and performance characteristics.

1. Introduction

Digital logic gates form the fundamental components of contemporary electronic circuits, essential for binary data processing in different applications, from microprocessors to memory devices [1]. In the pursuit of designing more efficient and reliable digital circuits, the accurate characterization and analysis of these gates are paramount. The current paper explores the systematic design, simulation, and analysis of two universal logic gates such as NAND and NOR, utilizing Cadence Virtuoso software in conjunction with the ADE L environment [2]. The simulation process is orchestrated within the ADE L environment, a robust tool for circuit simulation and analysis [3]. Using transient analysis with a 200 ns simulation time, we gain insight into the dynamic behaviour of the gates over time. The resulting graphical data showcases how the gates respond to various input signals. These output graphs are not only crucial for understanding the gates' operational characteristics, but are also instrumental in assessing their performance, speed, and reliability in various digital applications [4]. In this study, we initiated the process by configuring CMOS transistors in Cadence Virtuoso version IC6.1.5.500.15, utilizing a PMOS length of 100 nm and a finger value of 1, depicted in Figure 1(a). Similarly, an NMOS configuration with a length of 100 nm and a finger value of 1 is illustrated in Figure 1(b).

The PMOS and NMOS finger widths were set at 250 nm and 120 nm, respectively, with total widths of 250 nm and 120 nm for PMOS and NMOS, respectively [4], forming the foundation upon which the gate structures were built. The design process involves the development of basic CMOS circuits for the NAND and NOR gates, featuring two input pins (i.e. A and B) and one output pin (Out) [5]. These circuits, constituting the primary building blocks of the gates, are precisely created within the Cadence Virtuoso environment [5].

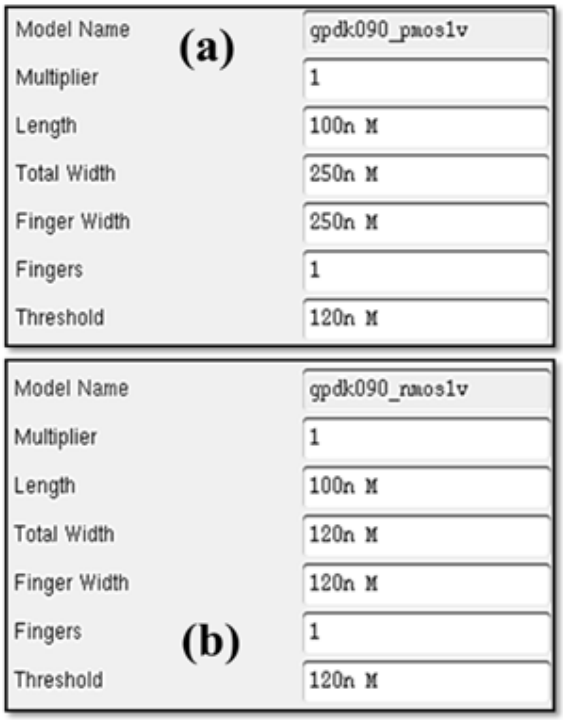


Figure 1: (a) Quality metric of considered PMOS, (b) Quality metric of considered NMOS.

Cadence Virtuoso is a critical EDA tool for custom circuit design and analysis in MOS technologies, particularly within CMOS VLSI. It supports RFIC, photonic IC, and system-in-package module design, allowing layout edits within the context of all ICs on a module or other fabrics like chips, modules, and boards. VLSI primarily serves in designing electronic components such as microprocessors and memory chips, creating integrated circuits by integrating millions of transistors [3-4]. Moreover, NAND and NOR gates in digital circuits are used as versatile Boolean gates that perform the logical operation of outputting [5-6]. This paper endeavours to establish and develop an innovative methodology that contributes to the advancement of designing NAND and NOR gate circuits and conducting transient simulations in Cadence Virtuoso software, with the objective of expanding existing knowledge in this domain. This research tutorial is constructed with the motive to providea clear image and description of how to carry out transient stimulation of NAND and NOR circuits using Cadence Virtuoso environment (ADE L) and will provide easy access to all the details for the creation and implementation of NAND and NOR gates without much hassle of web surfing.

2. Simulation consideration

Simulation is orchestrated in the ADE L environment, a powerful circuit analysis tool. We employ transient analysis with a 200 ns simulation time to observe the dynamic behaviour of the gates over time [6]. During this phase, additional pins are connected to the circuit schematic to enable the extraction of valuable output data, which includes input pins A and B, and the output pin 'Out' [7]. The resulting output data, capturing the gates' responses to different input signals, is presented in graphical form. For simulation, input pins (V_a and V_b) were linked to pulse voltage sources from the Cadence library's analog lib, with a maximum voltage limit of 1 V, streamlining the process [8], in addition to V_{CC} supply of 1 V dc bias voltage and 0 V of ground voltage. To facilitate ease of use and representation in electronic designs, symbols for each of the designed gates are generated using the cell view command and subsequently saved within the library alongside their respective schematics [9]. This ensures that the gates can be efficiently employed in the design and simulation of larger digital circuits [10] just like other components saved in the analog library and cadence main files for the transistors.

During the simulation of the gates, two pulse sources are employed, each characterized by a voltage profile consisting of two states: voltage I (0 V) and voltage II (1 V). These pulses are tailored to different periods and rise/fall times, with one pulse featuring a 60 ns period and the other a 20 ns period, both possessing rise and fall times of 50 ps. These input waveforms serve as the stimulus for the gates under study, enabling the observation of their responses to varying input conditions, and after simulation [11] through different environments, those waveforms can be plotted after selecting either transient analysis DC analysis, or AC analysis methods in the virtuous environments.

3. Results and discussion

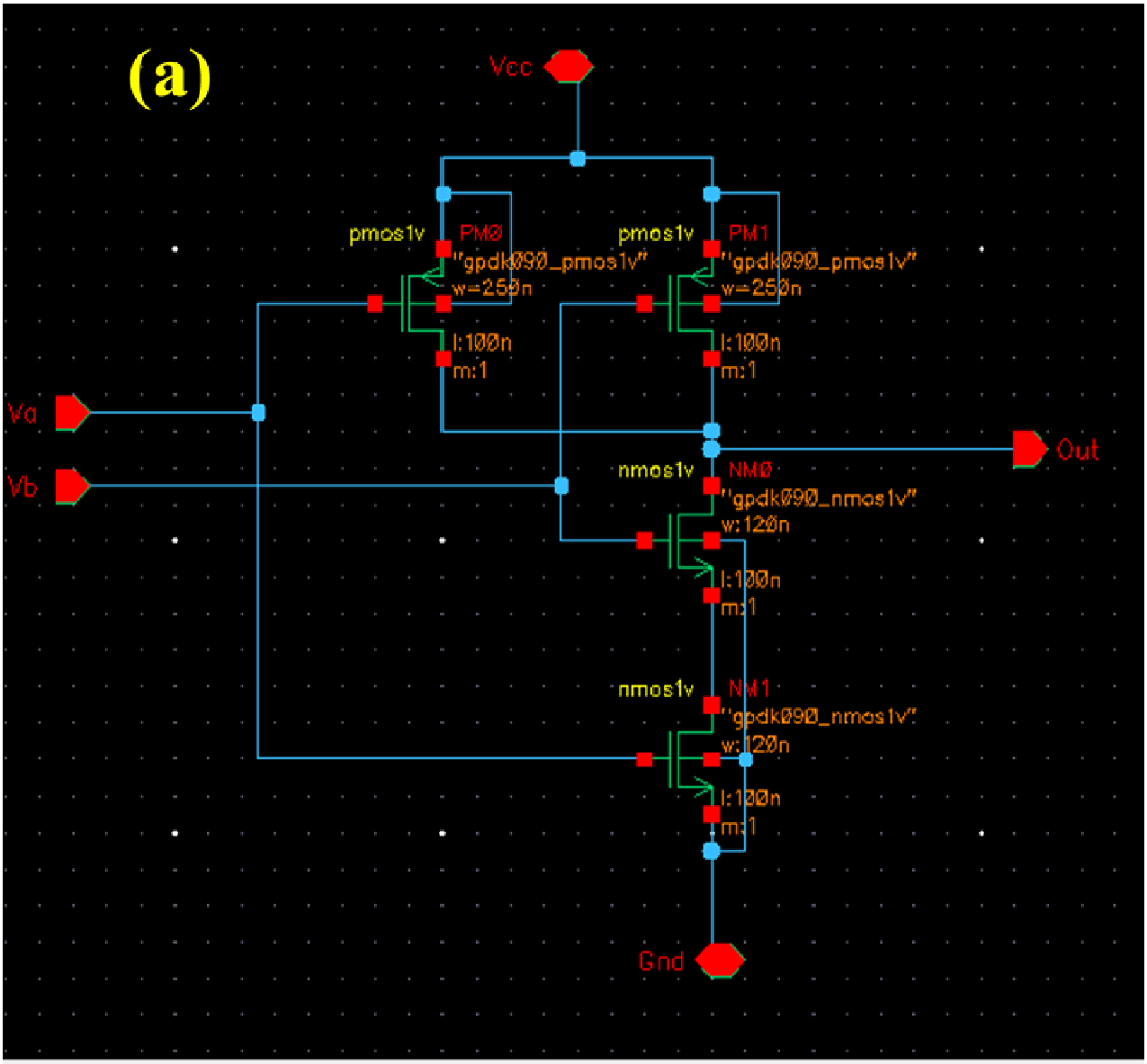
In our current undertaking, we have successfully implemented the making of NAND and NOR gates using Cadence Virtuoso version IC6.1.5.500.15, employing transient analysis with input pulse signals [12]. These gates exhibited the expected behaviour within the ADE L environment and we have opted for transient analysis for the outputs. The NAND gate outputs 'false' only when both inputs are 'true,' while the NOR gate produces a 'true' output if at least one input is 'false'. These versatile gates can serve as building blocks for all digital logic gates, encompassing NOT, AND, OR, XOR, and XNOR gates, enabling their application in digital circuits, arithmetic operations, data processing, memory design, digital systems.

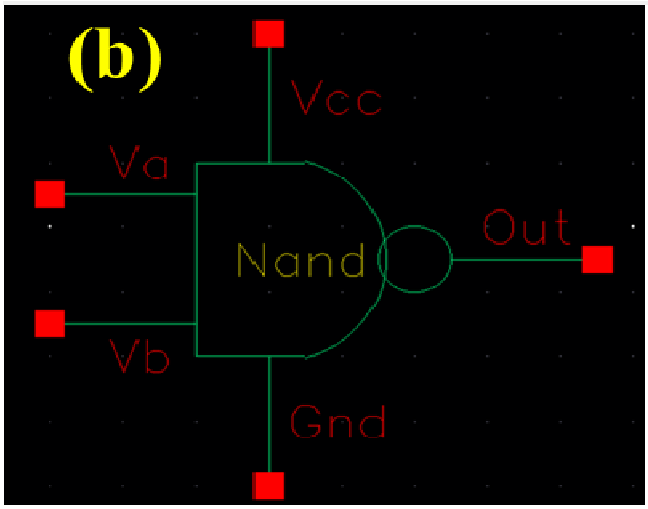
3.1 NAND gate

The NAND gate, a fundamental digital logic gate, executes the 'NOT-AND' operation and is recognized as a universal gate due to its capability to implement various basic logic gates efficiently (mentioned above) through appropriate connections. Two different pulses of values 60 ns period with a pulse width of 30 ns, and 20 ns period with a pulse width of 10 ns were collectively taken here for a comparative study, as shown in Figure 2. Moreover, the rise time and fall time were considered as 50 ps for both the considered cases utilizing complementary metal-oxide-semiconductor (CMOS) technology, NAND gates can be created with advantages like low power usage and rapid switching attributes [13]. In a CMOS NAND gate, complementary pairs of NMOS (n-channel metal-oxide-semiconductor) and PMOS (p-channel metal-oxide-semiconductor) transistors are used to achieve the desired logic function [14]. From the transient response, as depicted in Figure 3(b), we have seen that when both the inputs A and B (red and green pulses) are at logic level 0 (representing 'false' or 'off' state), the output 'Out' (pink colored) is at logic level 1 (representing 'true' or 'on' state) [15].

3.2 NOR gate

The NOR gate is a fundamental digital logic gate, executing the 'NOT-OR' operation. Regarded as a universal gate, like the NAND gate, it can implement other basic logic gates (AND, OR, NOT) through suitable connections through appropriate connections [16]. Like NAND gate, when either input A or B or both are at logic level 1 and the output 'Out' is at logic level 0. The NOR gate's output is the inverse of the OR operation, to put it differently [17]. Complementary CMOS technology allows NOR gates for digital circuits to be constructed and fabricated. It involves connecting complementary pairs of NMOS and PMOS transistors in a manner that facilitates the realization of the intended logic function, enabling efficient and low-power digital circuit design [18]. Here, NMOS transistors were connected in a parallel combination, however, PMOS transistors were connected in series, as shown in Figure 4. A NOR gate performs the logical operation of 'NOT-OR'. It takes two or more inputs and produces an output that is the reversal of the OR operation on those inputs. When both inputs to a NOR gate are low (0), the output is high (1). In all the other cases, the output is low (0). From the transient response (Figure 5(d)), it has been found that when both the inputs A and B (red and green pulses) are at logic level 0 (representing 'false' or 'off' state), the output 'Out' is at logic level 1 (representing 'true' or 'on' state) [19-20]. Similarly, if either input A or input B or both are at logic level 1, the output 'Out' remains at logic level 0 (marked in a pink colored curve).





(c)

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 2: (a) Schematic circuit diagram of NAND gate in Cadence Virtuoso software, (b) Symbol of NAND gate generated in Cadence, (c) Truth table of NAND gate.

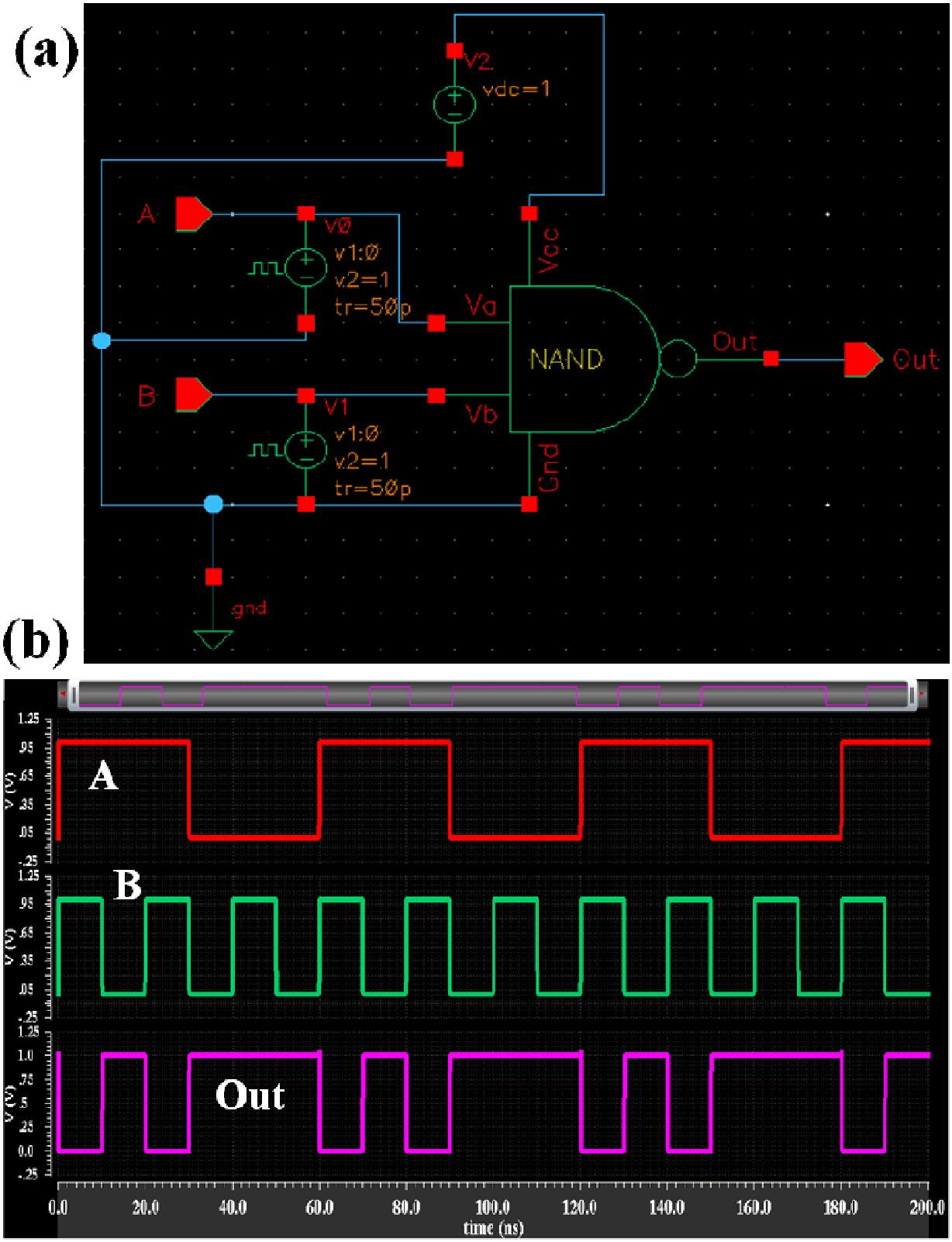


Figure 3: (a) Schematic of the simulation circuit of NAND gate, (b) Transient response of NAND gate.

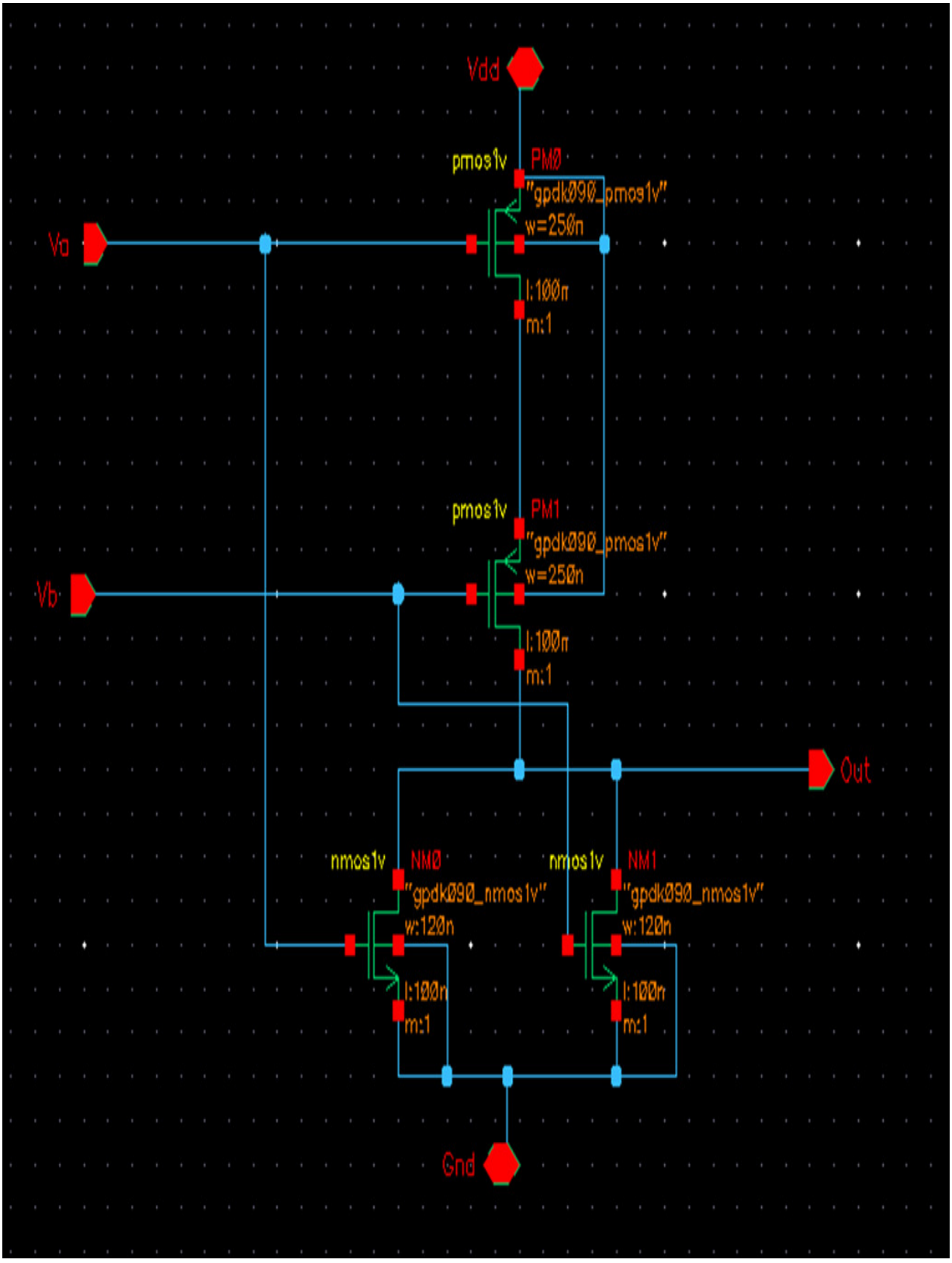
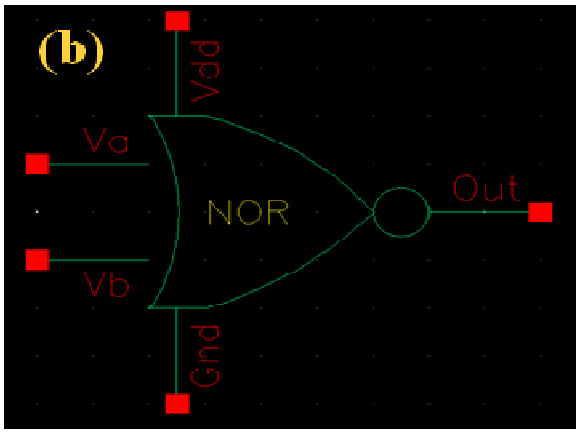
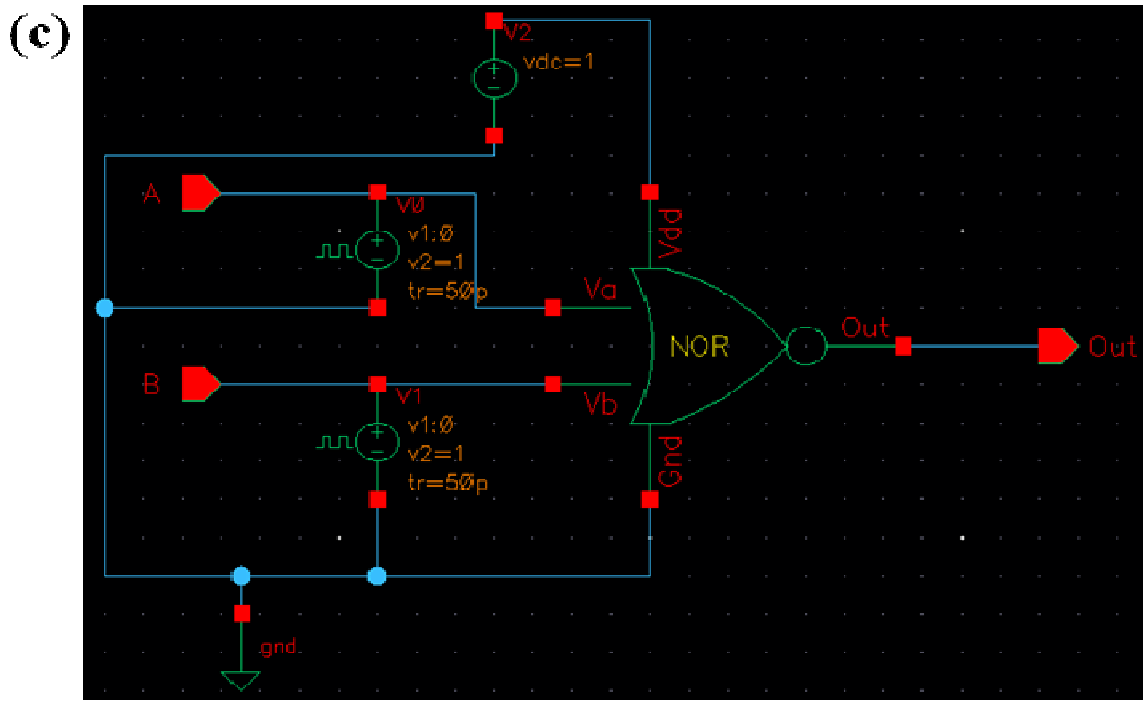


Figure 4: Schematic circuit diagram of NOR gate in Cadence Virtuoso software.

(a)

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0





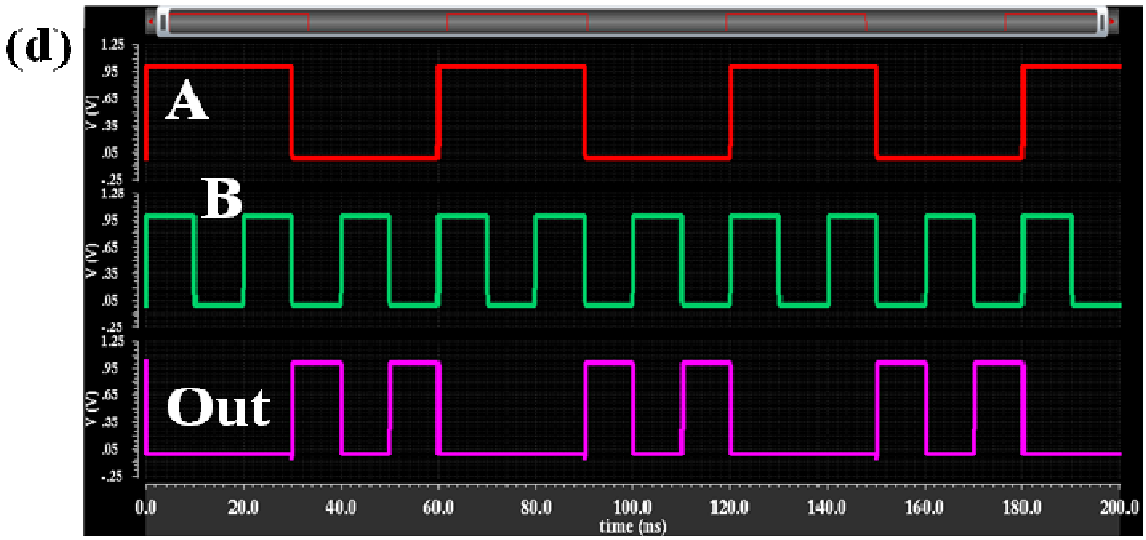


Figure 5: (a) Truth table of NOR gate, (b) Symbol of NOR gate, (c) Simulation circuit of NOR gate, (d) Transient response of NOR gate.

4. Conclusions

The design and simulation of NAND and NOR gates in Cadence Virtuoso have provided valuable insights into the behavior and functionality of these fundamental digital logic gates. This tutorial paper primarily focuses on the design of NAND and NOR gate employing Cadence Virtuoso (ADE L) with a 90 nm technology node, where PMOS and NMOS length was considered as 100 nm, and the widths for PMOS and NMOS were taken as 250 nm and 120 nm, respectively. The transient analysis was carried out for the duration of 200 ns in Cadence Virtuoso. Both these logic gates showed accurate output based on their Truth table, which indicated the functional correctness of the logic gates. A detailed tutorial has been provided here, which represents how to design, and simulate NAND and NOR gate circuits in Cadence Virtuoso in addition to their transient analysis.

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