RP Current Trends In Engineering And Technology
Vol. 3, No. 2 (April – June 2024) pp. 23–29
e-ISSN: 2583-5491

RESEARCH PLATEAU PUBLISHERS

Cite this article: I. Maity, A. Majumdar, Computation of key analog circuit parameters employing different topological configuration of current mirror circuits: A comprehensive analysis of gain, noise, and power consumption, *RP Cur. Tr. Eng. Tech.* **3** (2024) 23–29.

Original Research Article

Computation of key analog circuit parameters employing different topological configuration of current mirror circuits: A comprehensive analysis of gain, noise, and power consumption

Indranil Maity[1,*], Aheli Majumdar[2]
[1]Department of Electronics and Communication Engineering (ECE), Institute of Engineering and Management (IEM), Kolkata, University of Engineering and Management (UEM), Kolkata, India
[2]Department of Electronics and Communication Engineering (ECE), Institute of Engineering and Management (IEM), Kolkata, India
*Corresponding author, E-mail: indrasanu026@gmail.com

ARTICLE HISTORY
Received: 27 June 2024
Revised: 14 August 2024
Accepted: 16 August 2024
Published online: 19 August 2024

KEYWORDS
Cascode current mirror; Noise PSD; Gain; Power consumption; Cadence Virtuoso.

ABSTRACT
Cascode current mirrors simplify the designing of complex analog circuits with an aim to maximize the vital performance metrics, considered into the simulation. The present paper focuses on designing of three cascode current mirror circuits with a 5V DC supply voltage to attain notable AC gain values. The entire simulations were performed in Cadence Virtuoso with a 90 nm technology library. Here, we considered three different cases of cascode current mirror circuits viz. (a) Case 1: Differential pair with active current mirror having 5V input voltage, which produced gain of 8.76 dB, power of 509.6 pW, and noise power spectral density (PSD) of 0.97 μV^2/Hz, followed by (b) Case 2: Differential pair with active current mirror having 1.5V input voltage, which developed gain of 14.98 dB, power of 509.6 pW and noise PSD of 24.58 μV^2/Hz, and finally, (c) Case 3: Unity gain buffer circuit, which generated the aforementioned parameters as 0.37 dB, 36820 pW and 31.70 μV^2/Hz, respectively. Different parametric simulations were conducted such as AC analysis to calculate the gain, noise analysis, and the computation of power consumption in the ADE L environment. Additionally, statistical simulation (DC analysis) was also performed to observe the circuit's characteristic outputs. Comparison of the results indicated that the second circuit configuration (Case 2) attained the highest AC gain (14.98 dB), followed by the first, and third configurations. Moreover, the first and second circuit configurations demonstrated the lowest power consumption (509.6 pW). Furthermore, the first configuration (Case 1) also exhibited the lowest noise PSD, indicating minimal distortion compared to others.

1. Introduction

Any chip that uses differential transmission reduces its vulnerability to interference and noise-induced signal corruption. Nonetheless, the need to convert a signal from differential to single-ended frequently arises eventually, and this is where current mirrors (CM) come into play. CM are current regenerating circuits, which can sense current through input branch, reproducing same current in the output branch, maintaining the current magnitude irrespective of load at the output. Besides replicating, CM can also amplify or attenuate reference current to output current. They are implemented in devices as one of the major preliminary blocks for integrated analog or a mixed-signal circuit, for instance, current-mode A/D converter, low-dropout regulator, operational amplifier, voltage level shifter, and analog filter, and so on, which in turn could be directly influenced by the performances of CM [1]. Being rudimentary building blocks, the way in which CM have been constructed dictates the general performance of these integrated circuits [2]. Cascode Current Mirrors (CCM), on the other hand, are modifications over the simple CM, aiming at enhancing crucial performance metrics. Voltage unity gain buffers or voltage followers are employed in today's cultivated analog and mixed signal circuits. Their principal role is to decrease or increase the impedance in a circuit, so they are very handy in almost every field from processing audio signals to interfacing sensors [3]. This is particularly with regard to the amplification of signals inside circuits, and thus it becomes essential to design unity gain buffer configurations, which are suitable to deliver positive gain, safeguarding the integrity of a given signal [4]. These configurations are most convenient in applications wherever signal strength must be increased without additional noise or distortion interfering with linearity.

Deo et al. [5] evaluated the use of active MOSFET load, Wilson current mirror, and Widlar current mirror circuits to analyze the implementation of a MOSFET differential amplifier (BiMOS differential pair), and observed that the diode connected topology yielded the highest common mode rejection ratio (CMRR) of 31.48 dB. Jendernalik et al. [2] proposed a voltage unity-gain zero-offset CMOS amplifier designed in a 180 nm CMOS technology, which achieved gain error 0.3% and power supply rejection ratio (PSRR) of 72 dB.

Xie et. al. [1] devised an active-input cascode current mirror that dissipated 40 μW power and exhibited a replication error of less than 1.4% compared to the identical setup using the traditional active-input technique [6]. Iqbal et al. [7] presented a simulation analysis of a folded cascode current source using a cascode current mirror, conducted within the cadence environment and compared to previous multisim simulations. The results exhibited general agreement in output resistance and bandwidth, with minor variations in saturation behavior.

Since CM contribute to performance enhancement of any circuit readily, designing efficient current mirror configurations is the need of the hour, and thus the objective too. Few attempts have been made involving the aforementioned necessity, using cascode current mirrors (CCM), aiming in evaluation of key analog parameters such as gain, supply voltage requirements, power consumption and different analyses [8]. Instead of a normal current mirror circuits, CCM can be used to create both a differential pair and a unity gain buffer since CCM usually offer superior performance benefits [9-10]. In unity gain buffers, they generally provide higher output resistance, improved linearity, extended bandwidth, and better PSRR, ensuring accurate signal replication with minimal distortion, enhanced stability, better gain, reduced noise and reduced power consumption. Similarly, in differential pairs, they enhance output resistance, linearity, CMRR, PSRR, and bandwidth, enabling accurate amplification and improved noise rejection, critical for high-performance analog signal processing, better gain reduced noise and reduced power consumption. This paper focusses on designing three different cascode current mirror configurations with a 5V DC supply voltage, using CADENCE Virtuoso with a 90 nm technology library, and obtaining competent values through detailed simulation, comparison and analysis of comprehensive analog parameters, in the flexible ADE L environment, for efficient circuit designing.

2. Circuit design methodology

Cadence Virtuoso stands at the forefront of Electronic Design Automation (EDA) software, serving as a comprehensive suite essential for the design and simulation of integrated circuits (ICs) [11]. Virtuoso offers a versatile platform for every stage of the circuit design process. The design of various topologies of cascode current mirror circuits is fundamental in analog integrated circuit designs [12].

Table 1: List of the transistors from the three proposed circuit with their length and width.

Transistor type	Transistor name	Transistor finger width (nm)	Transistor total width (nm)	Transistor length (nm)
PMOS	PM1	900	900	100
PMOS	PM0	120	120	100
NMOS	NM1	900	900	100
NMOS	NM3	120	120	100
NMOS	NM4	900	900	100
NMOS	NM0	120	120	100
NMOS	NM2	900	900	100

This section outlines the methodology of configuring the circuits using generic process design kit (gpdk) 90 library, or the 90nm technology. The gpdk 90 technology serves as a foundational framework for semiconductor design, offering a standardized set of components, models, and design rules essential for developing integrated circuits (ICs). The proposed circuit designs have been discussed. A description of the transistor sizes have been mentioned in Table 1.

2.1 Differential pair with active current mirror circuits

This includes the first and second circuitry with similar design. The gate terminals of two PMOS transistors named ‘PM0’ and ‘PM1’ were interconnected via a narrow wire. The source terminals of both ‘PM0’ and ‘PM1’ were connected to the ‘vdd’ pin, which was provided with a DC supply voltage of 5V. The drain terminal of ‘PM1’ was attached to the drain terminal of NMOS ‘NM1’ via a thin wire. The wire which connected the drain terminal of ‘PM1’ to the drain terminal of ‘NM1’ was attached to the wire connecting the gate terminals of ‘PM0’ and ‘PM1’. The bespoke output pin ‘Vout’ was connected by a thin wire to the one that connected the drain terminals of ‘PM0’ and ‘NM3’, and the drain terminal of ‘PM0’ was likewise connected by a thin wire to that of NMOS ‘NM3’. Both ‘PM0’ and ‘PM1’ had their substrate terminals shorted to the supply voltage. The gate terminal of ‘NM1’ was linked to the input ‘Vin1’. The gate terminal of ‘NM3’ was linked to the input ‘Vin2’. The substrate terminals of NMOS ‘NM1’, ‘NM3’, and ‘NM4’ were grounded. The source terminals of both ‘NM1’ and ‘NM3’ were interconnected via a thin wire, and this wire connecting the source terminals of ‘NM1’ and ‘NM3’ was connected to the drain terminal of ‘NM4’ via a thin wire. Another input pin ‘Vb’, for supplying bias voltage, was connected to the gate terminal of ‘NM4’, whose source was also grounded. The inputs ‘Vin1’ and ‘Vin2’ were supplied with pulse voltages. The DC schematics of the first two configuration are shown in Figure 1(a) and Figure 2(a). A single pulse voltage was applied to ‘Vin1 consisting of a 5V input voltage, with a 20 ns time span, 50 ps rise and fall periods, and a 10 ns pulse width, was applied. ‘Vin2’ was subjected to a pulse voltage applied with the following parameters: 5V input voltage, 60 ns time period, 50 ps rise and fall durations, and 30 ns pulse width. With the second arrangement, ‘Vin1’ received a single pulse voltage of 1.5 V, which had a 20 ns period, 50 ps rise and fall periods, and a 10 ns pulse width. ‘Vin2’ received a pulse voltage of 1.5 V with a duration of 60 ns, rise and fall periods of 50 ps, and and a pulse width of 30 ns.

2.2 Unity gain buffer circuit using current mirror

The gate terminals of two PMOS transistors named ‘PM0’ and ‘PM1’ were interconnected via a narrow wire. The source terminals of both ‘PM0’ and ‘PM1’ were connected to the ‘vdd’ pin, which was provided with a supply voltage of 5V. A thin wire was used to connect the drain terminal of ‘PM1’ to that of the NMOS ‘NM0’ terminal. The wire that linked the gate terminals of ‘PM0’ and ‘PM1’ was connected to the wire that connected the drain terminal of ‘PM1’ to the drain terminal of ‘NM0’. The customized output pin ‘Vout’ was connected by a thin wire to the one that connected the drain terminals of ‘PM0’ and ‘NM1’, and the drain terminal of ‘PM0’ was also connected by a thin wire to the drain terminal of NMOS ‘NM1’. Both ‘PM0’ and ‘PM1’ had their substrate terminals shorted to the supply voltage. The gate terminal of

'NM0' was linked to the input 'Vin'. Gate terminal of 'NM1' was connected to 'Vout'. The substrate terminals of NMOS transistors 'NM1', 'NM0', and 'NM2' were grounded. The source terminals of both 'NM1' and 'NM0' were interconnected via a thin wire, and this wire connecting the source terminals of 'NM1' and 'NM0' was joined to the drain terminal of 'NM2' via a thin wire. Another input pin 'Vb', for bias voltage supply, was attached to the gate terminal of 'NM2', whose source was also grounded. The DC schematic is shown in Fig. 3(a).A pulse voltage consisting of a 1µV input voltage, a time period equal to 20 ns, rise and fall times of 50 ps, an upper limit voltage of 1V, and a pulse width of 10 ns was delivered to the input 'Vin' [13].

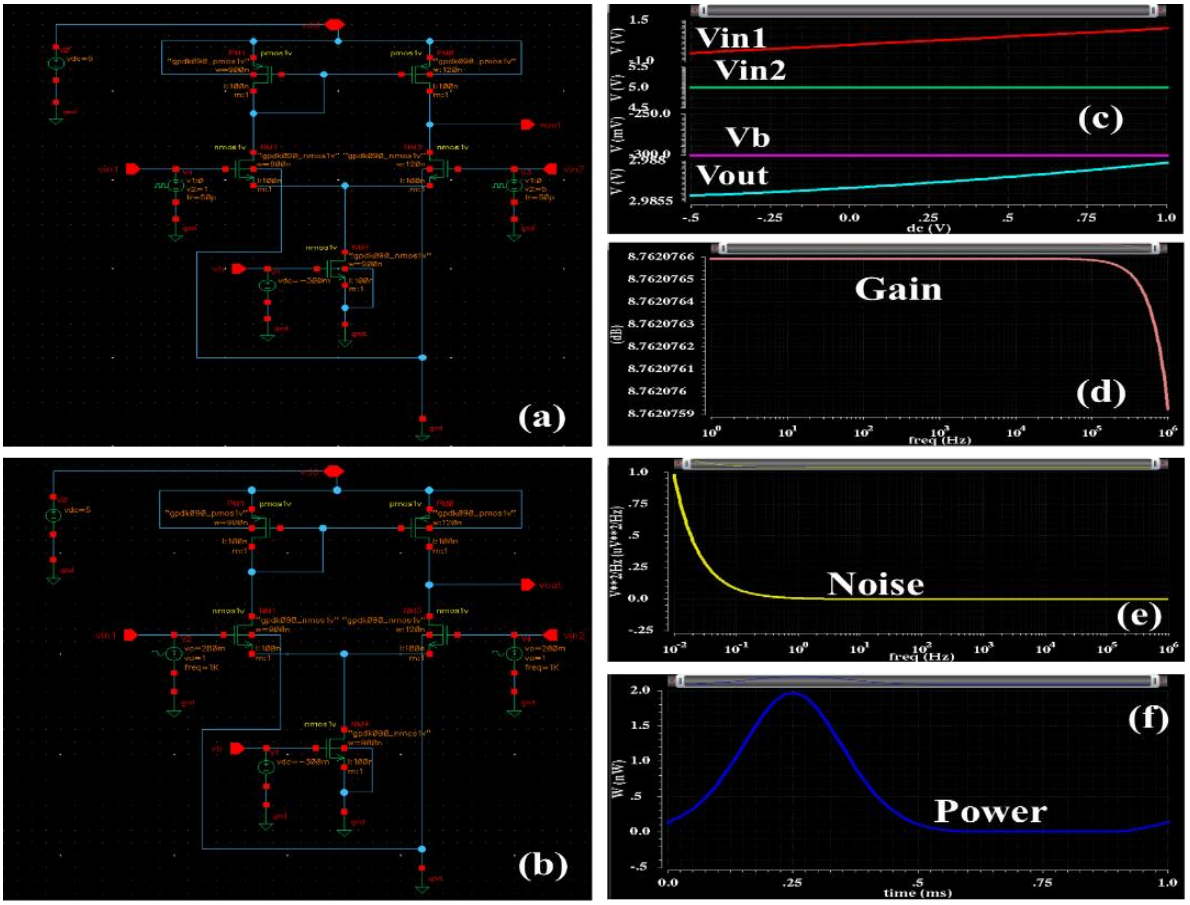

Figure 1: (a) Schematic of Differential pair with active current mirror circuit with DC pulsating input voltage of 5V; (b) Schematic of Differential pair with active current mirror circuit with AC sine input voltage of 5V; (c) DC output characteristics of the Differential pair with active current mirror circuit with DC pulsating input voltage of 5V; (d) Output AC gain characteristics of the Differential pair with active current mirror circuit with AC sine input voltage of 5V circuit; (e) Noise PSD characteristics of the Differential pair with active current mirror circuit with DC pulsating input voltage of 5V; (f) Power consumption characteristics of the Differential pair with active current mirror circuit with AC sine input voltage of 5V.

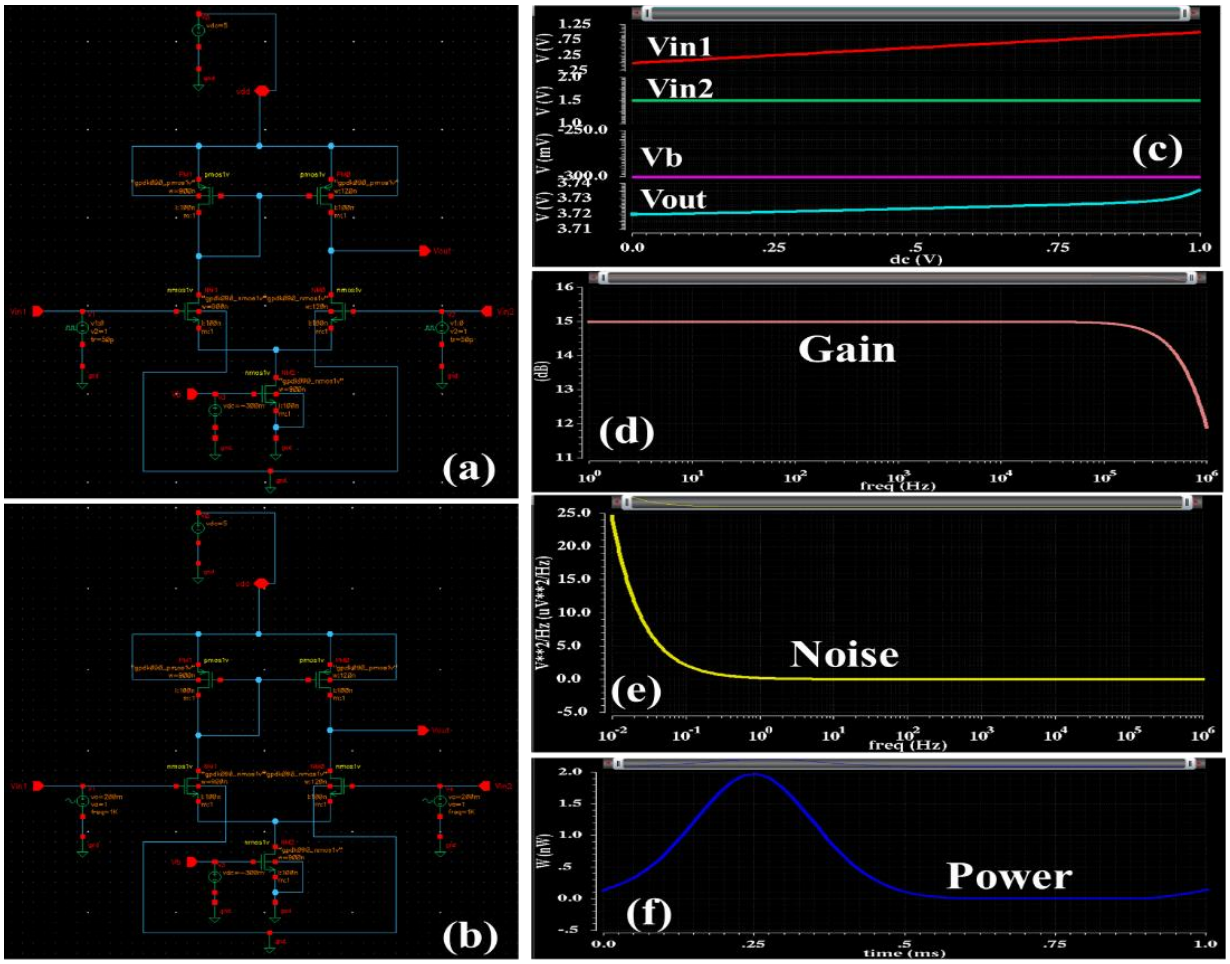

Figure 2: (a) Schematic of Differential pair with active current mirror circuit with DC pulsating input voltage of 1.5V; (b) Schematic of Differential pair with active current mirror circuit with AC sine input voltage of 1.5V; (c) DC output characteristics of the Differential pair with active current mirror circuit with DC pulsating input voltage of 1.5V; (d) Output AC gain characteristics of the Differential pair with active current mirror circuit with AC sine input voltage of 1.5V circuit; (e) Noise PSD characteristics of the Differential pair with active current mirror circuit with DC pulsating input voltage of 1.5V; (f) Power consumption characteristics of the Differential pair with active current mirror circuit with AC sine input voltage of 1.5V.

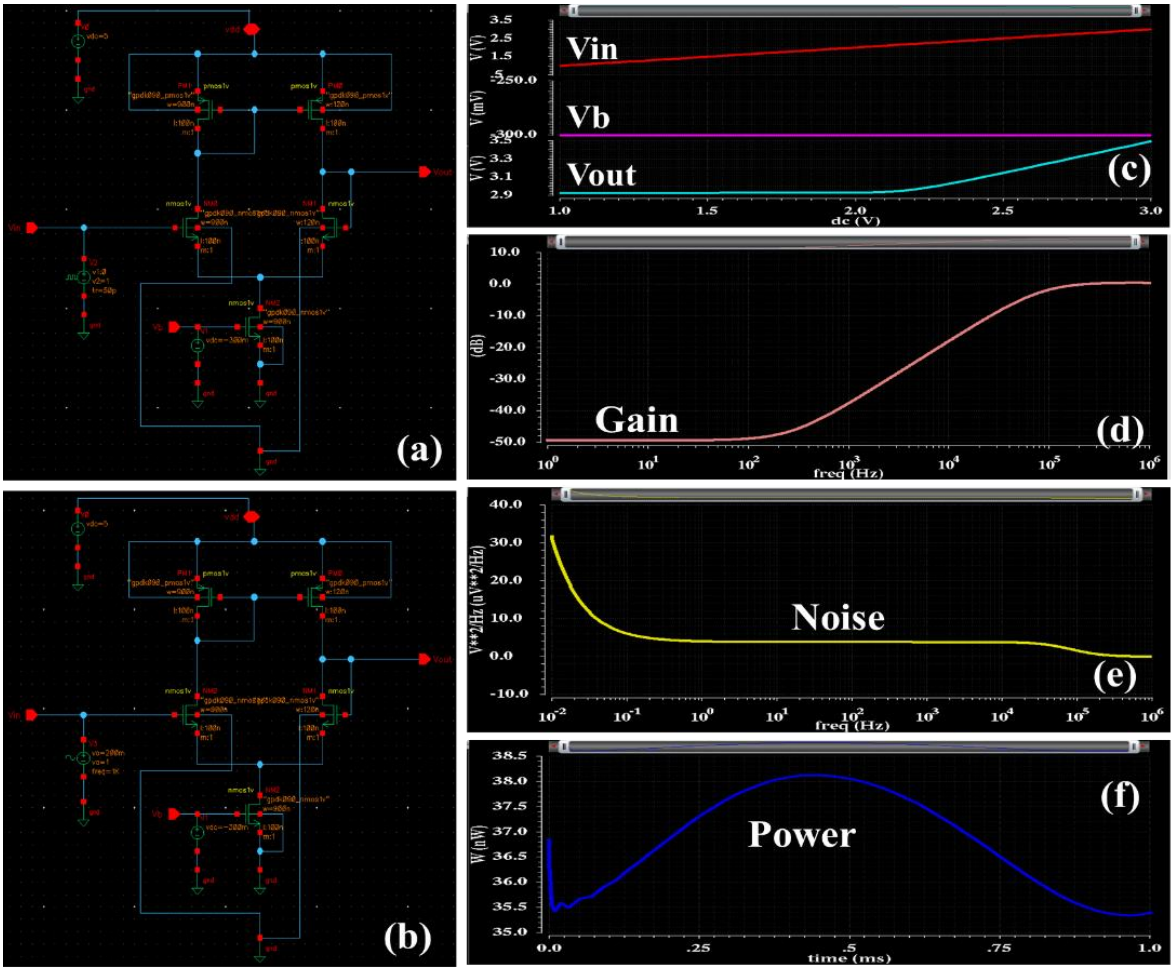

Figure 3: (a) Schematic Unity Gain Buffer circuit with DC pulsating input voltage of 1µV;
(b) Schematic of Unity Gain Buffer with AC sine input voltage of 1µV;
(c) DC output characteristics of Unity Gain Buffer with DC pulsating input voltage of 1µV;
(d) Output AC gain characteristics of the Unity Gain Buffer circuit with AC sine input voltage of 1µV;
(e) Noise PSD of the Unity Gain Buffer circuit with DC pulsating input voltage of 1µV;
(f) Power consumption characteristics of Unity Gain Buffer circuit with AC sine input voltage of 1µV.

3. Simulations

This section presents simulation and parameter specifications of the three discussed current mirror configurations, designed using CADENCE Virtuoso tool, using GPDK90 (or the 90 nm) technology [13]. DC analysis was carried out for obtaining the input-output behaviour [12]. The DC supply voltage was fixed at 5V. The necessary offset voltages and bias voltages were fixed for 200 mV and -300 mV, respectively. The pulse voltages were attached to simulate DC analysis of the curve, but for AC analysis, instead of pulse voltage, sine voltage was applied. AC schematics for the three circuitry are depicted in Figure 1(b), Figure 2(b) and Figure 3(b) correspondingly in sequence. For sine voltage sources, frequency range was employed between 1 Hz and 1 MHz; AC magnitude and amplitudes both were set at 1V and AC frequency of 1 kHz was provided. In case of the 1st configuration, the input sine voltage was set to 5V for both the input pins, 'Vin1' and 'Vin2'.

For the second circuitry, the input sine voltage was set to 1.5V for both the input pins, 'Vin1' and 'Vin2'.For Vin1, phase was set to 0 and for Vin2, phase was set to 180 degrees, in both the configurations. For the third circuit design, the input DC voltage was set to 1µV and phase was fixed at 0 degree. The sweep type was set to Logarithmic, and 500 steps were assigned. During noise analysis, to calculate noise PSD, frequency ranges were changed to operate between 10 mHz and 1 MHz. Number of points per decade were selected to be 100. Output pin was selected as the positive output noise, and ground terminal was selected as the negative output noise. During power consumption, transient analysis was chosen with 1 ms simulation time. All the mentioned parameters were fixed for all the three circuits after repeated simulations with various experimental values, and all the simulations were orchestrated in ADE L environment.

4. Results and discussion

This module presents simulation results and the analogies of the three CCM proposed, making use of the ADE L environment. The results of the DC analysis are depicted in Figure 1(c), Figure 2(c) and Figure 3(c) correspondingly in sequence. Results of AC gain, noise analysis for noise PSD and power consumption have been discussed below. A comparison of the obtained results have also been made in Table 2.

Table 2: Comparison of the input voltages and output parameters obtained.

Circuit No.	Input Voltage (V)	Gain (dB)	Power (pW)	Noise PSD (μV²/Hz)
1	5	8.76	509.6	0.97
2	1.5	14.98	509.6	24.58
3	0.000001	0.37	36820	31.70

4.1 Differential pair with active current mirror and realistic current source circuit

The resulting positive AC gain (Figure 1(d)) was computed to be 8.76 dB, which indicated enhanced circuit performance. During noise analysis calculations (Figure 1(e)), noise PSD was obtained as 0.97 $\mu V^2/Hz$, which was of the lowest order, since it provided better CMRR and maintained high trans-conductance, contributing to the stability and reliability of the circuit, minimizing the risk of interference and distortion. It also indicated improved Signal-to-Noise ratio (SNR), resulting in better clarity, enhanced sensitivity, and expanded dynamic range. The power consumed (Figure 1(f)) was received as 509.6 pW. The total current in the circuit was equal to sum of the currents through the two transistors, therefore the circuit was able to maintain a balanced operation. Experimentally, this was very low power, showcasing an efficiently designed circuit, reducing heat dissipation and maintained thermal stability, and improving reliability and longevity by preventing thermal-induced failures.

4.2 Differential pair with active current mirror and realistic current source circuit, with 1.5V applied to both the inputs

The resulting positive AC gain (Figure 2(d)) was computed to be 14.98 dB, which was of paramount significance, being the highest value obtained, ensuring that even small input signals can be amplified to a detectable level without significant distortion. This was due to increased trans-conductance, preserving the fidelity of the signal, enhancing the signal-to-noise ratio (SNR), guaranteeing improved performance in the long run. While performing noise analysis calculations (Figure 2(e)), noise PSD value was obtained as 24.58 $\mu V^2/Hz$, which was of lower order than the third circuit, but much higher than the 1st configuration. The power consumed was received the same as first circuit (Figure 2(f)). Even with reduced input voltage, the circuit was able to maintain a balanced operation, removing all common-mode variations, and leading to identical power consumption.

4.3 Unity gain buffer circuit using current mirror

The resulting positive AC gain (Figure 3(d)) was computed to be 0.37 dB. It being the lowest among the three configurations, indicated that the circuit only slightly amplifies the input AC signal, often desirable in applications where excessive amplification could lead to distortion or saturation. Being a configuration with only one input pin, reduced input voltage reduced the trans-conductance but increased the output resistance, thereby reducing the gain. During noise analysis calculations (Figure 3(e)), noise PSD value was obtained as 31.70 $\mu V^2/Hz$, which was the greatest among the three, due to a substantial rise in the flicker noise, leading to lower trans-conductance, providing comparatively poor signal reproduction. Such a high value indicated that the circuit was subjected to a significant amount of noise power over a given frequency range, affecting circuit performance and reliability detrimentally. This also lead to reduced SNR, and crosstalk, distorting signals. The power consumed (Figure 3(f)) was received as 36820 pW, which was comparatively very high, which can be a disadvantage and is adopted at the peril of lowering the energy productiveness of the entire arrangement. The circuit had only one input pin, therefore due to reduced input voltage, it drew more current to maintain a balanced and stable operation. It supported the circuit-energy inefficiency, paving a way for faster degradation of the circuit.

5. Conclusions

In this paper, three cascode current mirror-based circuits were designed and optimal parameter values were obtained through their analysis. The entire simulations were performed in Cadence Virtuoso version IC6.1.5.500.15 with a 90 nm technology library. Since current mirrors are commonly employed in the semiconductor industry, they were investigated in the study. Parametric simulations, including evaluations of gain, noise, and power consumption were carried out in the ADE L environment. Furthermore, DC analysis and other statistical simulations were run to assess the circuits' distinctive outputs. A comparison of the data showed that the second circuit configuration obtained the largest AC gain (14.98 dB), followed by the first and third configurations. As the first and second circuit configurations had the lowest and identical power usage (509.6 pW), it was discovered that they were more efficient than the third. Additionally, the first setup had the lowest noise PSD (0.97 $\mu V^2/Hz$) and consequently least distortion when compared to the other configurations. This research provided insightful information about the capabilities and features of cascode current mirrors. From the competent values obtained, it is possible to design future circuits that are even more efficient, thereby improving circuit performance. Additionally, effective power management solutions for electronic devices could be improved; portable device battery life extensions could be tested; and sensor interfaces could be further enhanced.

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