RP Current Trends In Engineering And Technology
Vol. 3, No. 2 (April – June 2024) pp. 40–45
e-ISSN: 2583-5491

RESEARCH PLATEAU PUBLISHERS

Cite this article: I. Maity, A. Dey, A novel approach to design combinational digital system blocks (demultiplexer and encoder) based on reversible logic gates, *RP Cur. Tr. Eng. Tech*. **3** (2024) 40–45.

Original Research Article

A novel approach to design combinational digital system blocks (demultiplexer and encoder) based on reversible logic gates

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ARTICLE HISTORY
Received: 30 July 2024
Revised: 14 August 2024
Accepted: 16 August 2024
Published online: 19 August 2024

KEYWORDS
Demultiplexer; Encoder; Reversible logic gates; Verilog, Garbage outputs; Quantum cost.

ABSTRACT
The present paper focuses on the implementation of two vital combinational digital systems viz. demultiplexer and encoder following some new design approaches with the help of reversible logic gates (one to one correspondence between I/P-O/P vectors). The proposed designs were hybrid in nature having different reversible logic gate (RLG) components compared to unitary RLG element. The entire simulations were performed using Verilog hardware description language in Xilinx Vivado 2018.2 simulator. Here, the investigation was performed on (i) designing of 1:4 demultiplexer (demux) using two NFT (New Fault Tolerant gate) RLGs (with 3 I/Ps and 3 O/Ps parity level), and one TKS RLG with the same 3*3 parity level. While, the second one was the implementation of 8:3 encoder using seven URG RLGs (with 3*3 parity level), and one Twin SJ RLG (with 5*5 parity level). The first configuration (1:4 demux) comprised of two gate level (GL) stages, where the first GL stage consisted of one TKS RLG, and the second GL stage had two NFT RLGs, thus the overall design had three number of RLGs. Moreover, the second configuration (8:3 encoder) consisted of three numbers of GL stages, where the initial stage contained of two URGs (universal reversible gates) and one Twin SJ RLG. Additionally, the second and third GL stages comprised of three URGs, and two URGs, respectively. Hence, the design had total eight number of RL gates. The following key parameters were computed here for both the considered cases (i.e., demux and encoder) viz. ancilla inputs, garbage outputs, quantum cost, and hardware complexity. It was observed that the first configuration had three number of garbage outputs, while the second case had fifteen garbage outputs. All the results were analyzed to compare the performance metrics against the existing reversible systems. Implementation of such kind of combinational logic circuits are of great use in different critical applications like communication systems, serial to parallel converters, optical computing, quantum computing along with an aim of minimal heat dissipation, and low power consumption.

1. Introduction

Reversible logic has become a vital research area in the development of low-power digital designs due to its potential applications in quantum computing, optical computing, and nanotechnology. Unlike traditional logic gates, reversible logic gates ensure a one-to-one mapping between input and output vectors, allowing the recovery of input information from the outputs and thereby reducing power dissipation [1]. This property makes reversible logic gates ideal for applications requiring energy efficiency, such as arithmetic operations, combinational circuits, and components for quantum computers. As the demand for energy-efficient and high-performance computing systems grows, the focus on reversible logic becomes increasingly significant, driving the development of innovative designs and methodologies. Combinational digital systems play a crucial role in various computing and communication technologies. Among these, demultiplexers and encoders are vital components that enable efficient data routing and encoding processes. The motivation for exploring reversible logic gates in designing combinational digital systems, such as demultiplexers and encoders, arises from the inherent advantages of these gates in reducing power consumption and enhancing system efficiency. Traditional designs often experience significant energy losses due to their irreversible nature, leading to heat dissipation and reduced performance. Reversible logic gates mitigate these issues by ensuring minimal energy loss. Notable improvements in energy efficiency and fault tolerance are done in order to design demux [2]. By employing reversible logic gates, the proposed designs aim to capitalize on these benefits, creating more efficient and robust digital systems and contributing to advancements in sustainable and scalable computing technologies [3].

Numerous researchers have investigated the application in various digital circuits of reversible logic gates. Garipelly et al. [1] provided a comprehensive review of reversible logic gates and their implementations, emphasizing their advantages in

digital circuit design. Kole et al. [4] proposed a novel algorithm for constructing demultiplexers and quantum multiplexers using the Universal Fredkin Gate, highlighting the versatility of reversible logic in complex digital systems. Rohini and Rajashekar [5] designed basic combinational circuits using reversible logic, demonstrating potential reductions in power consumption and performance enhancement. Recently, Kalamani et al. [6] designed encoders and decoders using reversible logic gates, further validating the practicality and efficiency of these gates in modern digital applications. These studies collectively illustrate the growing interest and ongoing efforts in integrating reversible logic into digital circuit design, paving the way for innovative low-power computing solutions. Numerous researchers have investigated the application in various digital circuits of reversible logic gates. Thabah and Saha [7] explored new design approaches for reversible BCD encoders using Feynman and Peres gates, demonstrating significant advancements in encoding techniques. Das and De [8] focused on the designing and implementing the reversible priority encoders using quantum-dot cellular automata, highlighting the potential of reversible logic in achieving high-performance digital systems. Shukla et al. [9] proposed a novel approach to designing decimal to BCD encoders with reversible logic, showing the practicality and efficiency of these designs in modern digital applications [10]. These studies collectively underscore the growing interest and ongoing efforts in integrating reversible logic into digital circuit design, paving the way for innovative low-power computing solutions.

Building on the existing research, this work presents a novel approach to designing a 1:4 demultiplexer and an 8:3 encoder using RLGs. Here the proposed designs utilize a combination of New Fault Tolerant (NFT) gates, TKS gates, Universal Reversible Gates (URG), and Twin SJ gates to achieve high efficiency and reliability. The 1:4 demultiplexer is structured in two gate-level stages with a minimal quantum cost and three garbage outputs, ensuring efficient signal routing based on selection inputs. The 8:3 encoder, organized into three gate-level stages, employs a combination of URG and Twin SJ gates, resulting in accurate binary encoding with low power consumption and fifteen garbage outputs. These designs not only demonstrate the practical application of reversible logic in complex digital systems but also highlight significant improvements in energy efficiency and fault tolerance, contributing to the advancement of low-power digital design.

2. New design approaches and verilog simulations

2.1 Considered designs

In the current design of the 1:4 demultiplexer and 8:3 encoder, several types of reversible logic gates (RLGs) are employed. These gates are chosen for their ability to maintain a 1:1 correspondence among input and output vectors, which is crucial for minimizing energy loss and heat dissipation. The specific reversible gates used in these designs are New Fault Tolerant (NFT) gate, TKS gate, Universal Reversible Gate (URG), and Twin SJ gate (Figure 1).

One TKS gate with 3 I/Ps and 3 O/Ps parity level and two NFT gates with the same 3*3 parity level were used to design a demux. TKS was used for its simple structure, which made easier to implement and NFT was used for the capability of detecting and correcting single faults. Seven URG gates with 3*3 parity level and one Twin SJ gate with 5*5 parity level were used to design an encoder. URG gates were used to implement a broad range of logical functions, and Twin SJ gate was used to implement more complex functions.

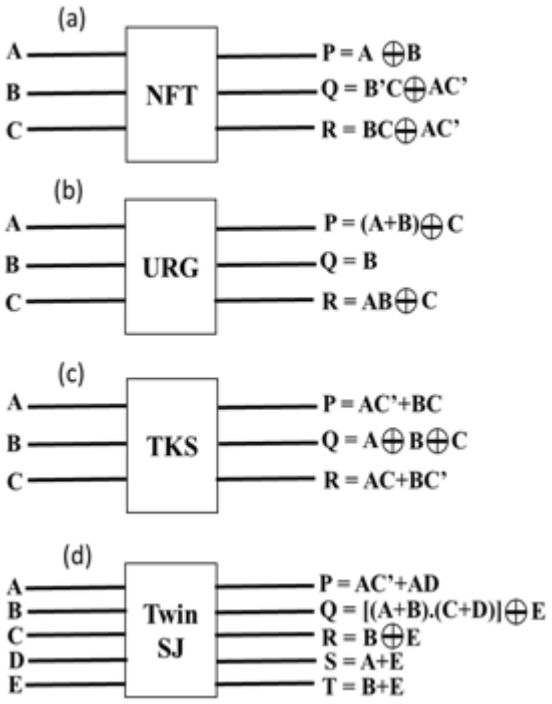

Figure 1: Four types of reversible gates- (a) NFT; (b) URG; (c) TKS; (d) Twin SJ.

2.2 Proposed methodology

2.2.1 Designing of the 1:4 demultiplexer (Demux)

The design of the 1:4 demultiplexer is structured using a combination of New Fault Tolerant (NFT) gates and a TKS gate, each featuring a 3x3 parity level is shown in the Figure 2. The demultiplexer is arranged in two distinct gate-level (GL) stages. The first GL stage employs a single TKS gate. This gate is responsible for initially processing the input signals, ensuring they are routed correctly based on the selection inputs. The TKS gate, known for its simplicity and efficiency, sets the foundation for the subsequent stage by handling the preliminary selection logic.

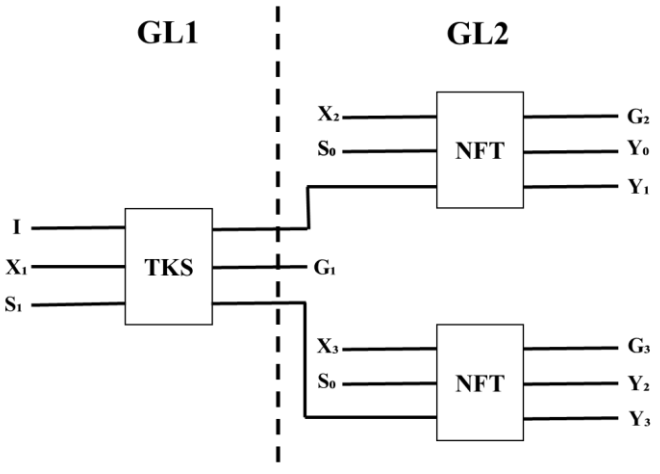

Figure 2: Designing of 1:4 demultiplexer.

In the second GL stage, two NFT gates are employed. These gates receive the processed signals from the first stage and further refine the routing based on the selection inputs. The NFT gates are chosen for their fault-tolerant properties, which enhance the reliability and robustness of the demultiplexer. The design ensures that any single fault within the circuit can be detected and corrected, thus maintaining the integrity of the output signals.

The entire configuration is designed to produce three garbage outputs, which are additional outputs necessary to maintain the reversibility of the logic gates. These outputs do not carry useful information but are essential for ensuring that the system operates with minimal energy dissipation and heat production. The number of quantum gates needed for the implementation of the demultiplexer is the quantum cost, and the overall complexity of the hardware were meticulously evaluated to confirm the efficiency of the design.

2.2.2 Designing of the 8:3 encoder

The 8:3 encoder design is more complex, utilizing seven Universal Reversible Gates (URG) and one Twin SJ gate. The encoder is organized into three gate-level stages (Fig. 3), each with a specific role in the encoding process. The initial stage consists of two URG gates and one Twin SJ gate. The URG gates are versatile and capable of implementing a wide range of logical functions, making them ideal for the first stage of encoding. The Twin SJ gate, with its 5x5 parity level, handles more complex logic, ensuring that the input signals are appropriately prepared for further processing. The second stage of the encoder comprises three URG gates. This stage continues the encoding process by further refining the signals based on the input lines, ensuring that each input combination is correctly mapped to its binary representation. The versatility of the URG gates allows for efficient handling of the encoding logic, maintaining the integrity of the input-to-output correspondence. In the final stage, two URG gates are used. This stage completes the encoding process by producing the final binary outputs. The design results in fifteen garbage outputs, a trade-off necessary for maintaining the reversibility of the logic gates. These garbage outputs, while not carrying useful information, are crucial for ensuring the system's energy efficiency and low power consumption. The performance metrics, including quantum cost, the number of garbage outputs and hardware complexity, were thoroughly analyzed. Here the encoder's design was optimized to achieve low power consumption and high efficiency, making it suitable for applications in communication systems and quantum computing environments.

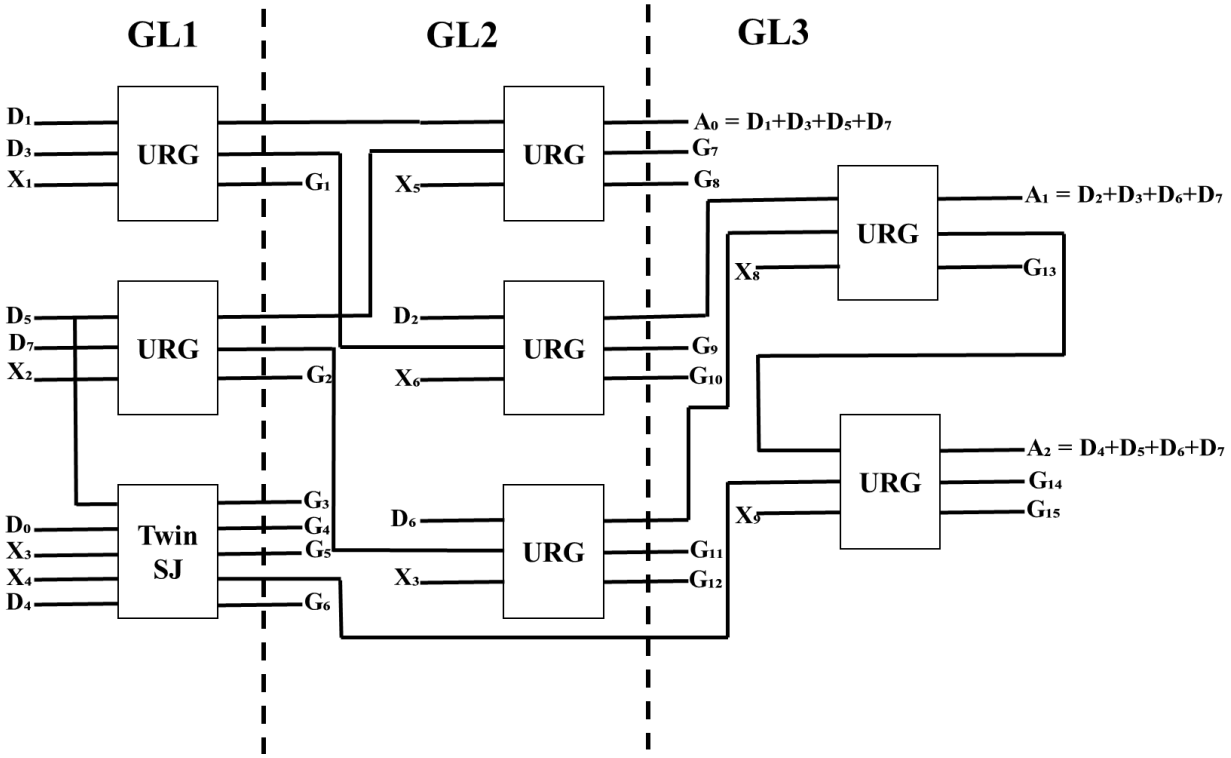

Figure 3: Designing of 8:3 encoder.

2.3 Verilog simulations

Both the 1:4 demultiplexer and 8:3 encoder designs were simulated using the Verilog hardware description language in the Xilinx Vivado 2018.2 simulator. The simulations were conducted to verify the correctness of the designs and to evaluate their performance metrics. The simulation results confirmed that the demultiplexer accurately routed the input signals to the appropriate output lines based on the selection inputs, as illustrated by the truth table. Similarly, the encoder successfully converted the active input lines into their corresponding binary codes, ensuring accurate encoding. The truth tables for both designs were used to ensure the correctness of the simulation results. For the demultiplexer, the selection inputs correctly determined the activated output line, while for the encoder, each input combination was accurately mapped to its binary output. The analysis of ancilla inputs, garbage outputs, hardware complexity, and quantum cost provided insights into the efficiency and effectiveness of the designs.

3. Results and discussion

3.1 Analysis on 1:4 demultiplexer

The Verilog simulation confirms that the demultiplexer functions correctly, gives the correct output signal with respect to the input signal and based on the selection line inputs. Key parameters like garbage outputs and ancilla inputs align with theoretical expectations. The truth table for the 1:4 demultiplexer shows the correspondence between the input selection lines and the activated output line. The Verilog simulation confirmed accurate routing of input signals based on selection inputs. The design produced three garbage outputs and maintained a minimal quantum cost, aligning with theoretical expectations.

Table 1: Truth Table of 1:4 demultiplexer.

Input	Select Lines		Output Lines			
I	S_0	S_1	D_0	D_1	D_2	D_3
I	0	0	1	0	0	0
I	0	1	0	1	0	0
I	1	0	0	0	1	0
I	1	1	0	0	0	1

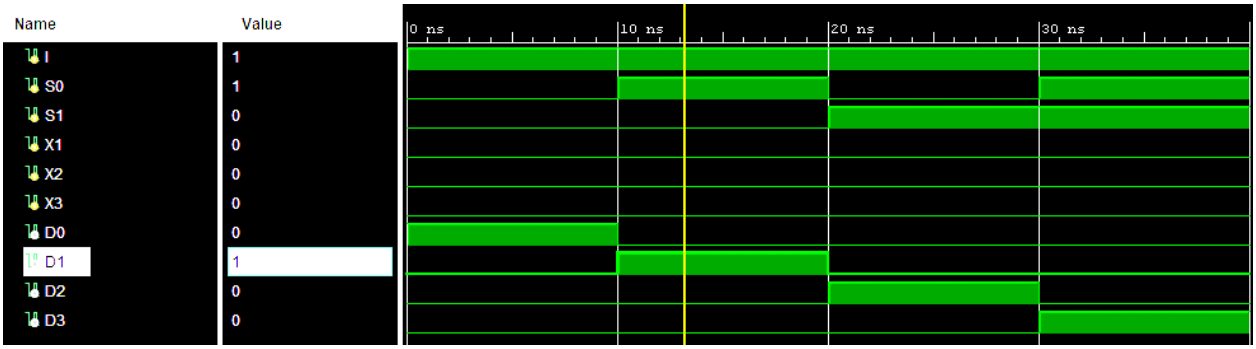

Figure 4: Simulated outputs of 1:4 demultiplexer.

The demultiplexer in the Figure 4 with respect to Table 1 routes the input signal A to one of the four outputs based on the selection lines S0 and S1. Here's how the circuit operates for different combinations of S0 and S1:

1. When S1=0and S0 = 0: The input A is routed to output Y0.
2. When S1=0 and S0=1: The input A is routed to output Y1.
3. When S1=1 and S0=0: The input A is routed to output Y2
4. When S1=1 and S0=1: The input A is routed to output Y3.

The TKS gate is responsible for processing the selection inputs S0 and S1 along with the data input A, ensuring the correct path is chosen for A. The NFT gates then complete the routing to the correct output line.

This demultiplexer design aims to implement and evaluate energy efficiency as one of it's core value. The main use of reversible logic gates in the demultiplexer design mainly reduces energy dissipation. Conventional logic gates lose energy through heat during bit erasures, that leads to considerable power inefficiency, specially in large-scale integrated circuits. This design evades this by ensuring that the computation is reversible, which means that no bits are lost and, as a result, minimal energy is dissoluted. Then comes the computational integrity of the device that lets RLGs preserve information, that makes the system less prone to errors generating from information loss. This trait is not valuable in systems where data integrity is at the highest range, such as cryptographic applications and high-precision computing jobs. The TKS and NFT gates in the demultiplexer make sure that the input information is perfectly routed to the correct output without any flaw. This demux design also has great applicability in low power systems. The minimization in power consumption and heat generation makes the demultiplexer design highly favourable for devices operating on battery and portable electronics. This is generally critical in medical devices, IoT sensors, and wearable technology, where extended battery life and reliability are important.

3.2 Analysis on 8:3 encoder

The Verilog simulation validates the correct operation of the encoder, accurately converting the active input line to its binary code. The truth table for the 8:3 encoder maps each input combination to its corresponding binary output. Performance metrics, including garbage outputs and ancilla inputs, were consistent with theoretical models. The encoder correctly converts multiple input lines into a binary representation.

Table 2: Truth Table of 8:3 encoder.

Input Lines								Output Lines		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1

0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

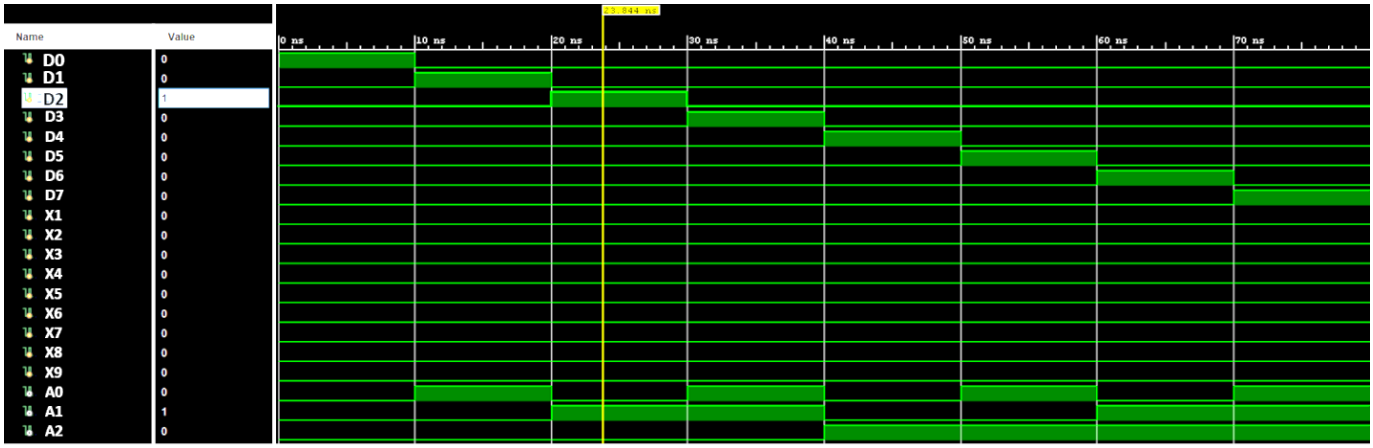

Figure 5: Simulated outputs of 8:3 encoder.

Here the simulation is shown in the Figure 5, where D2 is 1 and all the other inputs are 0, the value of the outputs are A0 is 1, A1 is 0 and A2 is 0 i.e, the output is 100. All the other outputs are also simulated and shown in the Table 2.The simulation validated the encoder's functionality, correctly converting input lines to binary codes with fifteen garbage outputs. The design demonstrated low power consumption and high efficiency, suitable for applications in communication systems and quantum computing. The encoder converts the active input signal into a binary code. For example, in the 4:2 encoder, only one input line is active (high) at any given time, and the output binary code corresponds to the position of this active input line. Here's how the circuit operates for different active inputs:

1. When Y0 is active (high): The output binary code is 00.
2. When Y1 is active: The output binary code is 01.
3. When Y2 is active: The output binary code is 10.
4. When Y3 is active: The output binary code is 11.

The URG gate processes the input signals (Y0, Y1, Y2, Y3) and generates intermediary signals that are then further processed by the Twin SJ gate. The combined processing by these reversible gates ensures the generation of the correct binary outputs (A0, A1).

Based on the above discussion, as the 1:4 demultiplexer design (based on reversible logic gates) uses a Toffoli gate (TKS) and two Fredkin gates (NFT). The quantum cost of this demultiplexer is calculated to be 15, stemming from the cost of one Toffoli gate (5) and two Fredkin gates (each with a cost of 5). The hardware complexity is relatively low, comprising only three gates. Additionally, this design does not require any ancilla inputs, maintaining simplicity, while ensuring the reversibility of the circuit. Likewise, the 8:3 encoder design based on RLG is constructed using seven Universal Reversible Gates (URGs) and a Twin SJ gate, which is treated as equivalent to two URGs. The total quantum cost of this encoder is estimated to be 36, considering each URG has a cost of 4, and the design utilizes seven URGs. The hardware complexity includes a total of 8 gates, reflecting the combined count of URGs and the Twin SJ gate. To facilitate the intermediate computations and ensure reversibility, the encoder requires four ancilla inputs, which help manage the interconnections and intermediate states across its three layers.

4. Conclusions

The study presents innovative designs for a 1:4 demultiplexer and an 8:3 encoder using reversible logic gates (RLGs).The proposed configurations demonstrate enhanced efficiency and performance, with reduced power consumption and heat dissipation compared to traditional systems. The designs utilize NFT, TKS, URG, and Twin SJ gates, giving key parameters like quantum cost, garbage outputs, and hardware complexity. Simulation results highlight the effectiveness of the proposed designs in various critical applications like communication systems and quantum computing. Here, the reversible logic gates are considered since it takes same number of inputs and outputs, which ensures significant reduce of energy loss. There is also potential for exploring the integration of these designs into more complex computing environments, paving the way for advancements in areas such as optical computing and advanced communication systems.

Acknowledgements

The authors are thankful to Institute of Engineering and Management (IEM) for providing support and facilities for the research work.

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