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Original Research Article

Impact of doping concentration on SOI structure to obtain high output current swing

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ABSTRACT
The work is focused to investigate the effect of doping concentration of substrate and source/drain region on the performance of Silicon-On-Insulator based devices. For this purpose, two MOSFETs structures are modelled and simulated using SOI in one of its layers in Silvaco TCAD device and process simulators. Doping profiles of both devices are varying to achieve maximum output current swing. On the basis of obtained results, it says that there is a significant increase in drain current from 2.4 mA to 2.8 mA when doping concentration of SOI structures varying from 1×10^{18} cm^{-3} to 1.7×10^{17} cm^{-3} in p-type region and from 1×10^{20} cm^{-3} to 1.1×10^{20} cm^{-3} in n-type region. Novel architectures and alternative substrates promise improvements in speed and power consumption.

1. Silicon-on-Insulator in MOSFETs

Silicon-on-insulator (SOI) technology is an important strategy for improving the performance of metal-oxide semiconductor field-effect transistors (MOSFETs) [1]. Figure 1 shows a structure of SOI on MOSFETs [2].

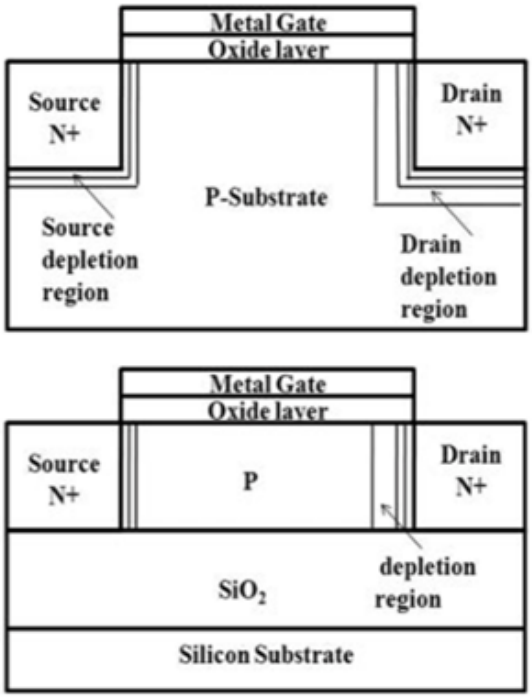

Figure 1: General structure of an SOI device.

The general design of an SOI-based MOSFET consists of mainly three layers, they are:

1. The top layer is Silicon layer, which is the active layer formed by the MOSFET channels.
2. The middle layer is the Buried Oxide layer (BOX), which is a protective layer that separates the top layer of silicon from the larger bottom layer of silicon. The BOX layer plays an important role in reducing parasitic capacitance, providing better isolated electricity and improving device performance.
3. The third layer is silicon substrate layer, acts as a mechanical support for the overall system and can also influence the thermal properties of the device [3].

The SOI design offers many advantages over more conventional MOSFETs. Like it reduced parasitic capacitance of the device using the BOX layer, allowing faster switching speeds. The electrical isolation of the prevents latch-up problems and allows for better packing density, improves specific integration and furthermore, reduced leakage currents. Therefore, SOI devices contribute to increased power efficiency. Furthermore, SOI MOSFETs exhibits thermal balance, providing greater reliability at elevated temperatures due to the effects of reduced leakage and automatic heating [4-6].

There are several parameters which can be modelled in SOI MOSFETs structure to optimize its performance, including doping amount, silicon layer thickness, buried oxide thickness, channel length, gate insulator material. Among these, doping concentration is especially important because it

affects threshold voltage, consequently carrier mobility and impact on the drain current [7]. The relationship between drain current (I_D) and doping concentration (N_D) is illustrate using the following equations:

$$V_T = V_{T0} + \frac{qN_D}{C_{ox}}(t_{si} - \Delta t_{si}) \quad (1)$$

where V_{T0} is the intrinsic threshold voltage, q is the charge of an electron, C_{ox} is the gate oxide capacitance, t_{si} is the silicon layer thickness, and Δt_{si} is the depletion width.

In the linear region, the drain current (I_D) is given by

$$I_D = \frac{\mu_o C_{ox}}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \quad (2)$$

where μ_n is the electron mobility, L is the channel length, V_{GS} is the gate –source voltage, and V_{DS} is the drain-source voltage. For saturation region, drain current is given as:

$$I_D = \frac{\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2 \quad (3)$$

Typically, as doping level increase, the threshold voltage also rises, which, in turn, impacts the drain current. By analysing and adjusting these factors, SOI MOSFETs can be optimized for various application, boosting both performance and efficiency in cutting-edge semiconductor technologies [8]. Despite the advantages, the SOI MOSFET model presents several technical challenges. The effects of reduced channel lengths are more pronounced in thin SOI layers, requiring stringent control over doping profiles and accurate modelling to maintain device performance. The buried oxide (BOX) layer can impede effective heat dissipation, resulting in self-heating phenomena that may degrade both the performance and reliability of the device. Additionally, quantum effects in ultra-thin SOI layers can influence carrier behaviour and threshold voltages, and variations in fabrication processes can cause notable difference in device characteristic [9].

This work focuses on the design and simulation of SOI MOSFETs utilizing established parameters in the ATLAS device simulation software [10]. After configuring these parameters, the doping concentration was systematically varied to analyze its effect on the device's overall performance. Comparative research found out upgrades and insights into how doping levels have an effect on the electric homes of SOI MOSFETs. Despite those blessings, the SOI MOSFET version gives several demanding situations. The results of smaller channels are extra stated on thin SOI layers, so correct manage and modeling is needed. The BOX layer can intrude with warmth switch, inflicting thermal emissions that affect tool performance and reliability. In addition, quantum effects in extremely-skinny SOI layers can have an effect on carrier dynamics and threshold voltages, main to big differences in device houses because of production adjustments.

2. Literature review

From last few decades, several methods have been investigated in designing and modelling of SPI structure. Literature Insights presents a summarized review of some of the popular works on Doping Concentration Variations in SOI Technologies.

Sandow et al. [11] experimentally investigated ultra-thin body SOI tunnel FETs. Using Wenzel-Kramer-Brillouin approximation, author focused on parameters such as channel length, gate oxide thickness, and source/drain doping concentrations. Results reveal negligible reliance on channel length but significant dependency on gate oxide thickness and doping concentration. The study correlates experimental findings with calculations based on a simple Landauer model, emphasizing the influence of bandgap narrowing and electrostatics on tunnel FET performance.

Mardiana et al. [12] explored integration of a phase modulator within an SOI rib waveguide structure with a p-i-n diode configuration. SILVACO software is utilized to predict electrical device performance under DC operation, revealing a correlation between increased doping concentrations and improved phase modulator efficiency, as indicated by decreased I_π values.

Wei-Yuan et al. [13] investigated the impact of doping concentration on the scaling of ultrathin SOI MOSFETs, demonstrating significant enhancement in the minimum scalable channel length for fully depleted (FD) SOI MOSFETs with doping. The integration of high-K dielectrics enables improved scalability towards the ITRS 45 nm technology node.

Bijender et al. [14] aims to investigate the effect of channel doping concentration and SOI layer thickness on the electrical behaviour of the device. Results indicate that decreasing channel doping concentration leads to a reduction in threshold voltage and improves saturation in the I_d-V_d curve. Additionally, decreasing SOI layer thickness results in reduced threshold voltage and sub-threshold swing.

Wen-Teng et al. [15] evaluated n-MOSFET reliability, considering doping concentrations and SOI configurations. PBTI testing highlights that high-doped devices induce significant tunneling leakage, with degradation linked to temperature, stabilizing over time. Thinner PD-SOI exhibits consistent threshold voltage and drive current under HCS, while FD-SOI better controls drain leakage compared to PD-SOI.

Bourahla et at. [16] reveals that nano-short DG-FinFET outperforms SG-FD-SOI-MOSFET in mitigating short channel effects (SCEs) and enhancing DC and RF performances. Using TCAD-SILVACO-Atlas simulator, optimal channel doping concentration is expected to enhance device efficiency further. DG-FinFET exhibits significantly reduced parasitic capacitances, resulting in enhanced cut-off frequency (ft) and maximum oscillator frequency (f_{max}), positioning it as a promising choice for RF applications and future device manufacturing advancements.

From above review, we can conclude that significant progress has been made in the fabrication technology of SOI (Silicon-On-Insulator), but there are still some issues need to be solved. The main problem with cannabis is the amount a grower can produce at reasonable costs in a large scale - and production will never be competitive when the processes taking place are so complex and moreover so expensive. High-quality LPCVD SiC is a slow process compared to other CVD processes and has thermal budget constraints from high-temperature processes as well, which restricts compatibility with other materials and process methods.

3. Device fabrication flow

The process to fabricate SOI MOSFETs starts with the growth or deposition of a high-quality silicon wafer substrate which will serve as the base or substrate for the device. A Buried Oxide (BOX) layer is then created using Separation by implanted oxygen or wafer bonding to electrically separate the top silicon layer from the bulk substrate and minimize parasitic capacitance. The top silicon device layer is then grown above the BOX layer which will provide the area where the active MOSFET regions will be formed. The next step is to design the doping profile for the source, drain and channel regions which specifies the types and concentrations of dopants to be implanted.

The gate structure is established by growing a thin gate oxide layer on the top silicon layer, followed by the deposition and patterning of a poly-silicon or metal gate electrode. The source and drain regions are doped through ion implantation or diffusion techniques. An annealing step is then performed to activate the dopants and mitigate any damage from the implantation process. Afterward, the source and drain regions are etched to form the electrical contacts for the device. The process simulation is conducted.

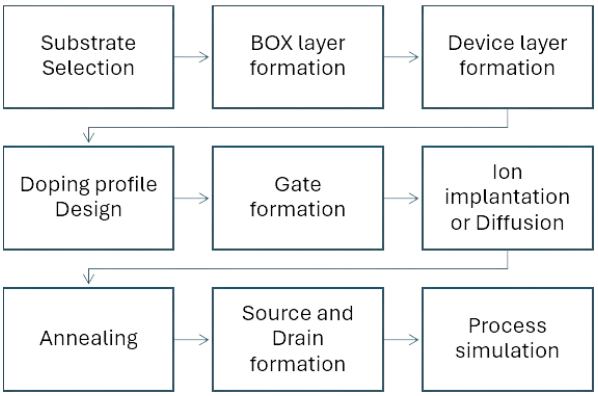

Figure 2: General fabrication process flow of MOS SOI.

4. Simulated results and discussions

The simulation of SOI MOSFET structures involves several key steps to model the electrical characteristics and analyse the impact of various parameters, such as doping concentration.

4.1 Device structure initializations

The process begins by defining the initial structure of the SOI MOSFET in the simulation software (e.g., ATLAS). This includes specifying the dimensions and material properties of the top silicon layer, buried oxide (BOX) layer, and the bulk silicon substrate.

4.2 Doping profile definition

Doping profiles are introduced for the source, drain, and channel regions. This step determines the nature and concentration of the dopants (e.g. boron for p-type and phosphorus for n-type) and their spatial distribution in the device.

4.3 Meshing and discretization

A mesh is generated for the tool structure to discretize the simulation domain. A finer mesh is usually used in regions with high gradients, along with the channel and close to junctions, to make certain accurate simulation effects.

4.4 Physical models activation

Relevant bodily models are activated to accurately capture the behavior of the device. This includes fashions for mobility, recombination, effect ionization, and quantum consequences if essential. These models account for the bodily phenomena that affect the tool overall performance.

4.5 Biasing and simulation execution

Appropriate biasing conditions are applied to the gate, source, and drain terminals to simulate the device operation. This includes placing the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) to simulate each the linear and saturation areas of operation. The simulation is then done to compute the electric traits which include drain present day (I_D) as opposed to gate voltage (V_{GS}) and drain present day (I_D) versus drain voltage (V_{DS}).

Table 1, shows the modelling parameters of basic SOI structure using standard parameters in ATLAS library and modified SOI, respectively.

Layer (thickness, doping concentration)	**Standard SOI MOSFET (Design1)**	**Proposed SOI MOSFET (Design 2)**
Silicon Substrate	60 nm, 1×10^{18} cm^{-3} p-type	60 nm, 1.7×10^{17} cm^{-3} p-type
Source/Drain Regions	20 nm, 1×10^{20} cm^{-3} n-type	20 nm, 1.1×10^{20} cm^{-3} n-type
Gate Oxide Layer	2 nm, SiO_2	2 nm, SiO_2

Figure 3, depicts the simulated results of the layered structure Design 2 (Include in Table 2).

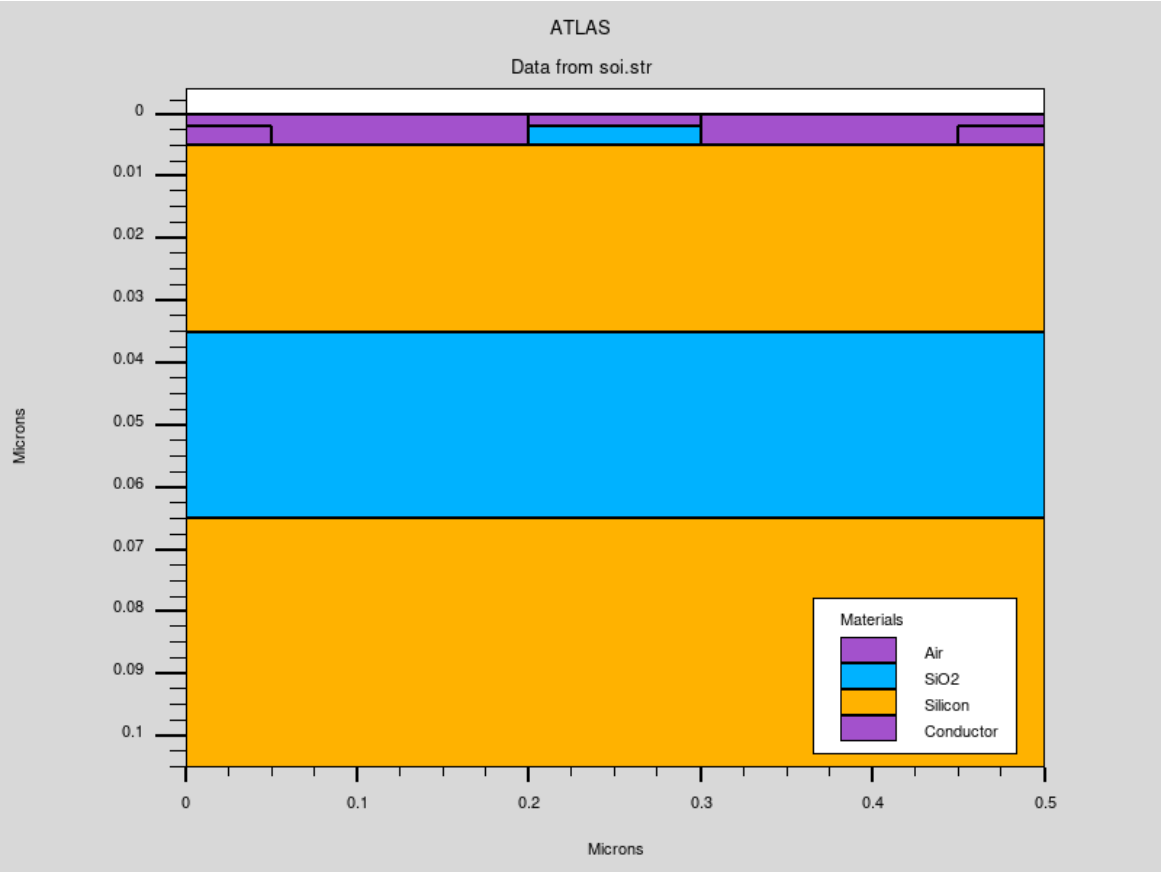

Figure 3: Process simulation SOI on atlas.

The results of the simulations for the basic SOI and modified SOI structures are illustrated in Figure 4(a) and Figure 4(b), respectively, showcasing their I-V characteristics.

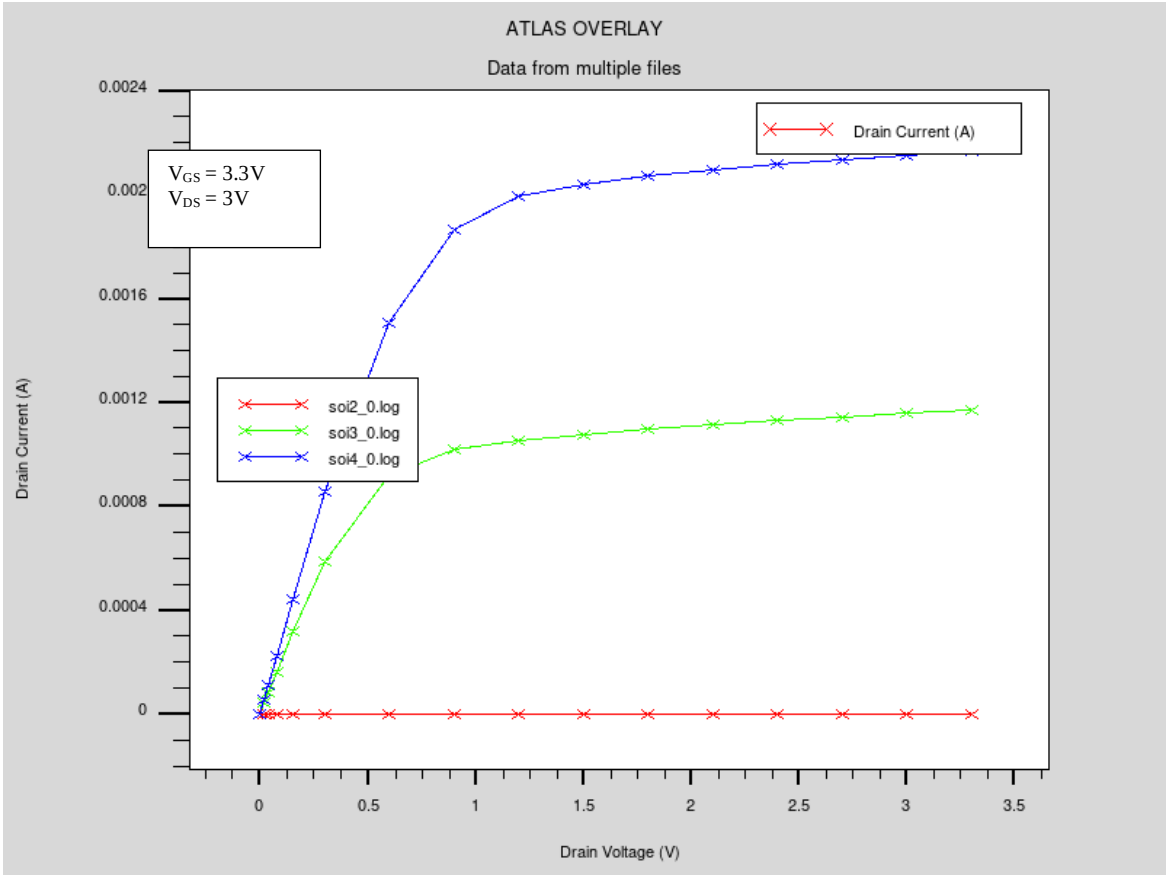

Figure 4(a): V-I characteristics curve of basic SOI on Atlas.

Figure 4(a) illustrates that basic SOI achieves a peak drain current of 2.4 mA under the conditions of V_{DS} = 3V and V_{GS} = 3.3V.

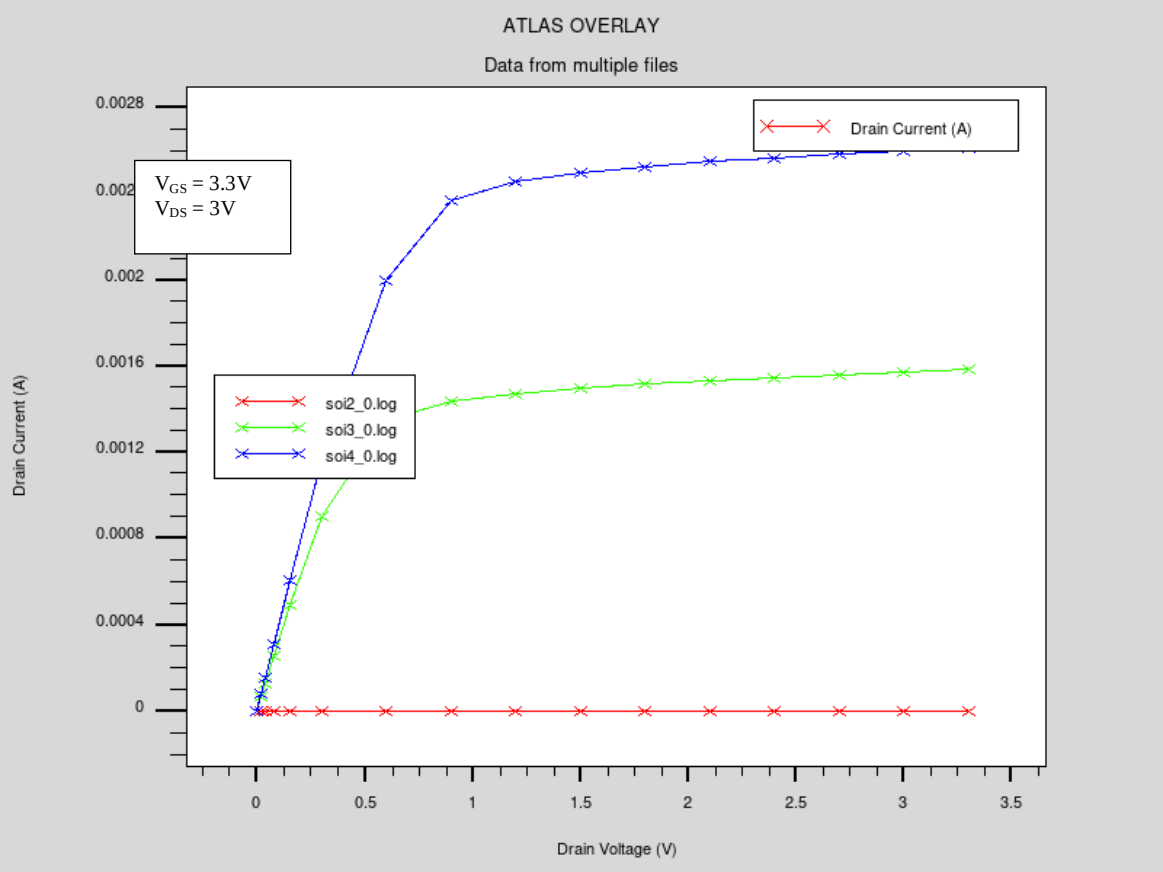

Figure 4(b): V-I characteristics of modified SOI on Atlas.

In Figure 4(b), it is demonstrated that modifies SOI attains a peak drain current of 2.8 mA under the conditions of V_{DS} = 3V and V_{GS} = 3.3V.

Hence, it can be inferred from Figure 4(a) and Figure 4(b) that modified SOI achieves significantly improved drain current. Table 2 presents a summary of the design specifications and performance attributes of basic SOI and modified SOI.

Table 2: Summary of SOI device design and their electrical properties.

SOI Substrate	Doping Concentration (cm^{-3})		I_{DS} (mA) At V_{GS} = 3.3V and V_{DS} = 3V
	p-type region	n-type region	
Basic SOI	1×10^{18}	1×10^{20}	2.4
Modified SOI	1.7×10^{17}	1.1×10^{20}	2.8

Table indicates that increasing drain current from basic SOI to modified SOI leads to enhanced drain current. Such devices exhibit the capability to drive substantial output current, improved carrier mobility and transconductance. Figure 5 shows the effect of variation of doping concentration on I_{DS}.

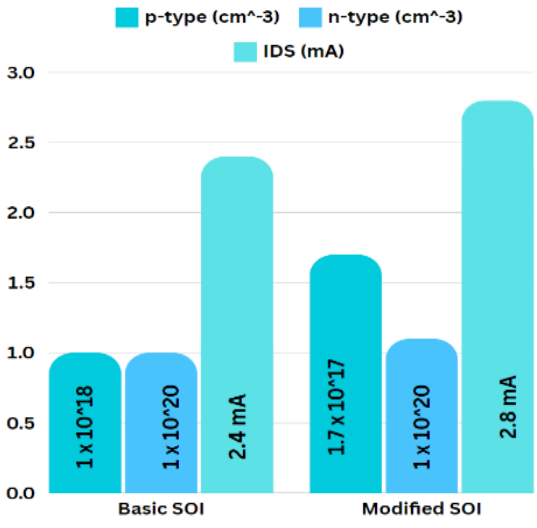

Figure 5: Variation of doping cocentration on I_{DS}.

5. Conclusions

By systematically increasing doping concentrations. Our investigation have revealed profound alterations in the characteristics of SOI Device. As we meticulously increased the doping concentration of p-type region from 1×10^{18} cm^{-3} to 1.7×10^{17} cm^{-3} and n-type region from 1×10^{20} cm^{-3} to 1.1×10^{20} cm^{-3}, notable enhancements were observed. These alterations resulted in a substantial augmentation in drain current, surging from 2.4 mA to 2.8 mA. Our empirical findings corroborate theoretical predictions, demonstrating that the increment in doping concentration yields amplified drain current.

6. Future scope

Exploring advanced material, integrating emerging technologies, and optimizing fabrication processes offer opportunities to enhance transistor performance. Novel architectures and alternative substrates promise improvements in speed and power consumption. Advanced simulations ans reliability assessments guide design, while interdisciplinary collaborations drives innovation to meet evolving electronics demands.

Authors' contributions

The author read and approved the final manuscript.

Conflicts of interest

The author declares no conflict of interest.

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Data availability

No new data were created.

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