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Review Article

Fabrication–integration co-optimization in advanced CMOS technology nodes

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ABSTRACT
The scaling of CMOS technology into the sub-10 nm regime has introduced fundamental physical, technological, and integration challenges that cannot be addressed through conventional geometric scaling alone. Device performance is now constrained by electrostatic limitations, variability, interconnect bottlenecks, and thermal effects. Consequently, a paradigm shift toward Fabrication–Integration Co-Optimization (FICO) has emerged, wherein fabrication processes and system-level integration strategies are jointly optimized. This paper provides a comprehensive analysis of FICO across advanced CMOS nodes, including FinFET, Gate-All-Around FET (GAAFET), and Complementary FET (CFET) architectures. Detailed discussions on fabrication challenges, integration bottlenecks, and co-optimization methodologies such as DTCO and STCO are presented. The work further explores emerging directions including machine learning-assisted process optimization and 3D heterogeneous integration, establishing FICO as a critical enabler of future semiconductor technologies.

1. Introduction

For over five decades, CMOS technology scaling has been the primary driver of advancements in microelectronics [1]. The historical trend of doubling transistor density approximately every two years has enabled exponential improvements in computational capability. However, as feature sizes approach atomic dimensions, traditional scaling principles encounter severe limitations [1,2].

At sub-10 nm nodes, electrostatic control degrades significantly, leading to increased leakage currents and reduced threshold voltage stability [3]. Moreover, fabrication variability at atomic scales introduces statistical fluctuations that directly impact device performance and yield. Simultaneously, interconnect delay has surpassed intrinsic device delay, fundamentally altering performance bottlenecks.

These developments necessitate a shift from isolated optimization of fabrication steps to a holistic co-optimization framework, where fabrication processes, device architectures, and system-level integration are designed concurrently. This concept, known as Fabrication–Integration Co-Optimization (FICO), forms the central theme of this work [4].

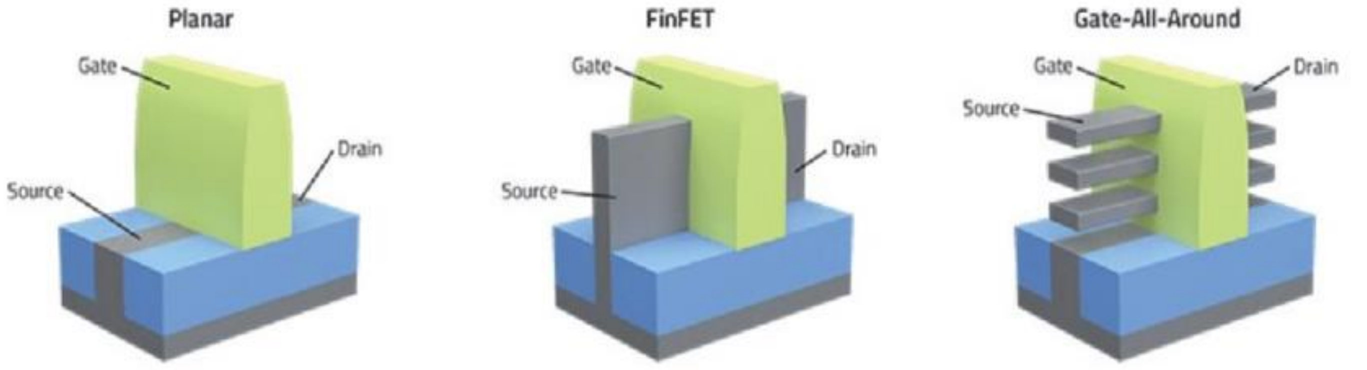

Figure 1: Evolution of CMOS technology showing transition from planar MOSFETs to FinFETs and GAAFETs [5,6].

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2. Limitations of conventional CMOS scaling

2.1 Electrostatic degradation and short-channel effects

As channel length decreases, the gate loses effective control over the channel potential. This results in phenomena such as Drain-Induced Barrier Lowering (DIBL) and subthreshold slope degradation [2,4,6]. The reduced gate control leads to increased off-state leakage currents, which significantly impact static power consumption.

In planar MOSFETs, the electric field from the drain extends into the channel region, lowering the potential barrier and allowing carriers to flow even when the device is nominally off. This effect becomes more pronounced as device dimensions shrink.

2.2 Variability and statistical fluctuations

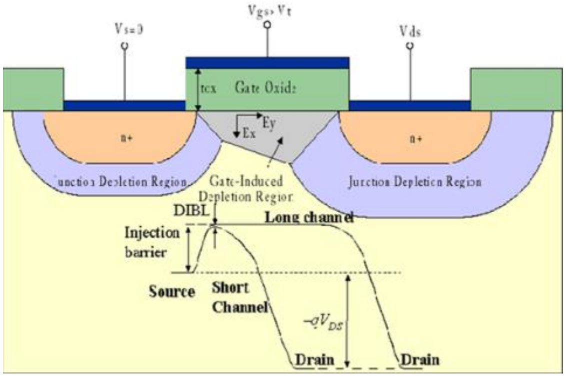
At nanometer scales, device behavior is increasingly governed by stochastic effects. Random dopant fluctuations (RDF), for example, lead to variability in threshold voltage due to the discrete nature of dopant atoms. Similarly, line-edge roughness (LER) introduces geometric variability that affects carrier transport [7].

Metal gate granularity further contributes to work-function variability, resulting in device-to-device performance inconsistencies. These variations complicate circuit design and necessitate guard-banding, reducing overall efficiency.

2.3 Interconnect bottlenecks

While transistor switching speeds have improved, interconnect performance has not scaled proportionally. The resistance of narrow metal lines increases due to electron scattering at surfaces and grain boundaries. Additionally, capacitance between closely spaced interconnects contributes to signal delay [8].

As a result, RC delay in the Back-End-of-Line (BEOL) dominates overall circuit performance, marking a fundamental shift from device-limited to interconnect-limited scaling.



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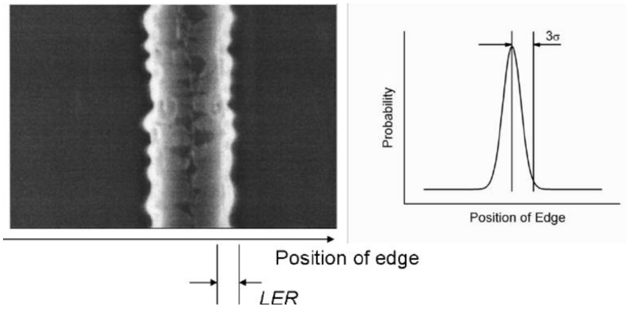

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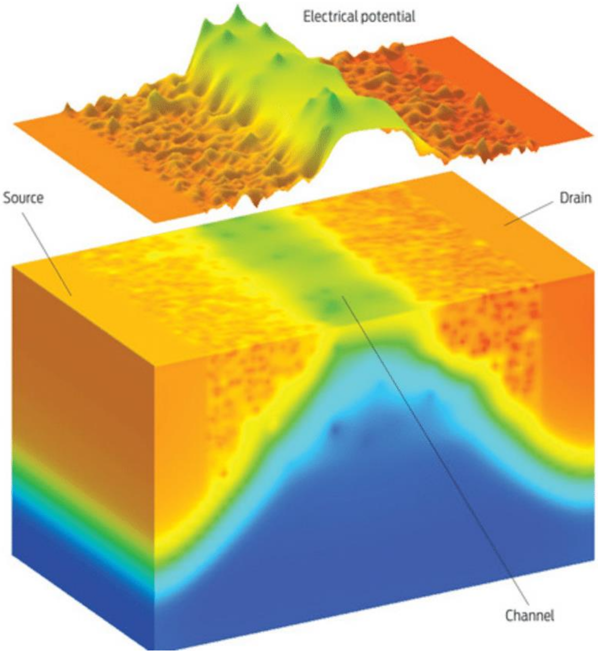

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Figure 2: (a) Key limitations of conventional scaling including short-channel effects [9], (b) line-edge roughness [10], and **(c):** random dopant fluctuations [11].

3. Fabrication–Integration Co-Optimization (FICO)

3.1 Conceptual Framework

FICO represents a unified optimization strategy that simultaneously considers [3, 5, 12]:

- Device fabrication processes
- Material selection
- Layout and design rules
- System-level architecture

Unlike traditional approaches, where fabrication and design are treated sequentially, FICO ensures that decisions in one domain are informed by constraints and opportunities in others.

3.2 Need for co-optimization

The complexity of advanced nodes arises from strong interdependencies between process steps and device performance [3,6,8]. For instance, modifying spacer thickness to reduce parasitic capacitance may affect strain engineering and carrier mobility. Similarly, layout constraints imposed by lithography directly influence circuit density and performance.

Thus, isolated optimization leads to suboptimal results, whereas co-optimization enables global performance improvements.

3.3 Relationship with DTCO and STCO

FICO integrates [7,12,13]:

- **DTCO**, which aligns process technology with circuit design
- **STCO**, which extends optimization to system architecture

Together, these methodologies enable cross-layer optimization from materials to systems.

4. Evolution of CMOS architectures

4.1 FinFET technology

FinFETs introduced a three-dimensional channel structure, improving gate control by wrapping the gate around multiple sides of the channel. This significantly reduces leakage and enhances scalability [6].

4.2 Gate-All-Around FET (GAAFET)

GAAFETs extend the concept further by surrounding the channel completely with the gate. Nanosheet-based GAAFETs allow precise control over channel width, offering design flexibility and improved electrostatics [5,6,13].

4.3 Complementary FET (CFET)

CFET technology stacks n-type and p-type transistors vertically, effectively doubling transistor density without increasing footprint. This represents a major step toward 3D integration [14].

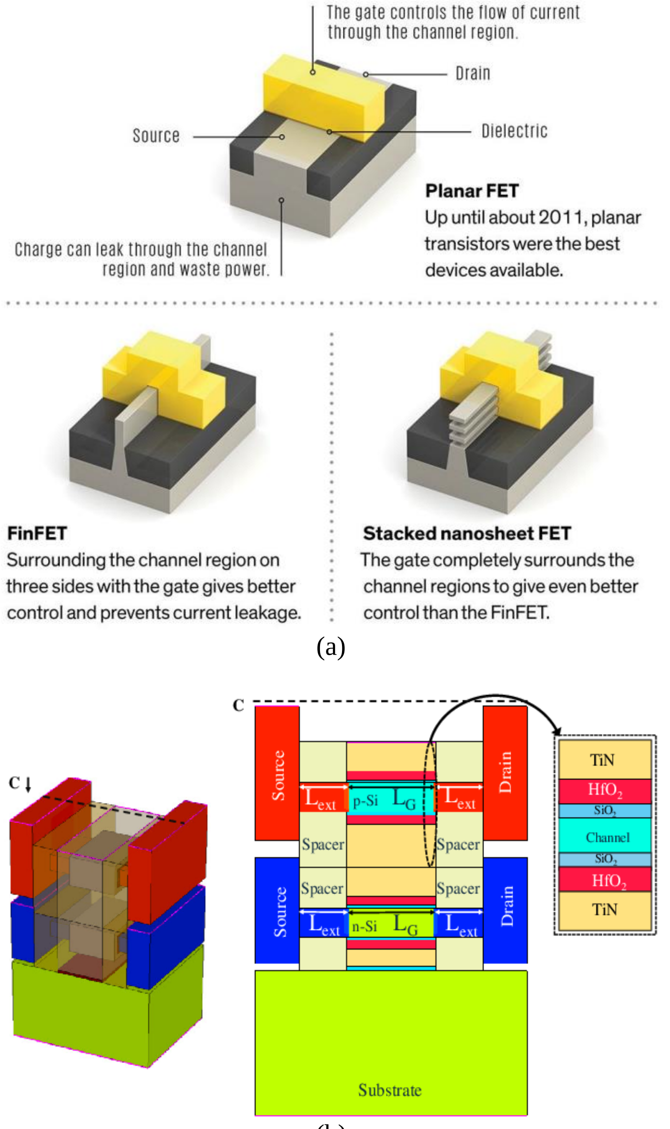

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Figure 3: (a) Comparison of planar MOSFET, FinFET, GAAFET, and CFET architectures highlighting structural evolution [15] and (b) electrostatic improvements [16].

5. Fabrication challenges at advanced nodes

Advanced CMOS fabrication requires atomic-scale precision. Extreme Ultraviolet (EUV) lithography introduces stochastic defects due to photon shot noise, leading to pattern variability [1,2,6]. Additionally, high-k dielectric integration must ensure uniform thickness and minimal interface defects [5]. Plasma processes used in etching can damage sensitive materials, affecting device reliability [7]. Furthermore, achieving uniform nanosheet thickness and spacing in GAAFETs requires highly controlled epitaxial growth and etching processes.

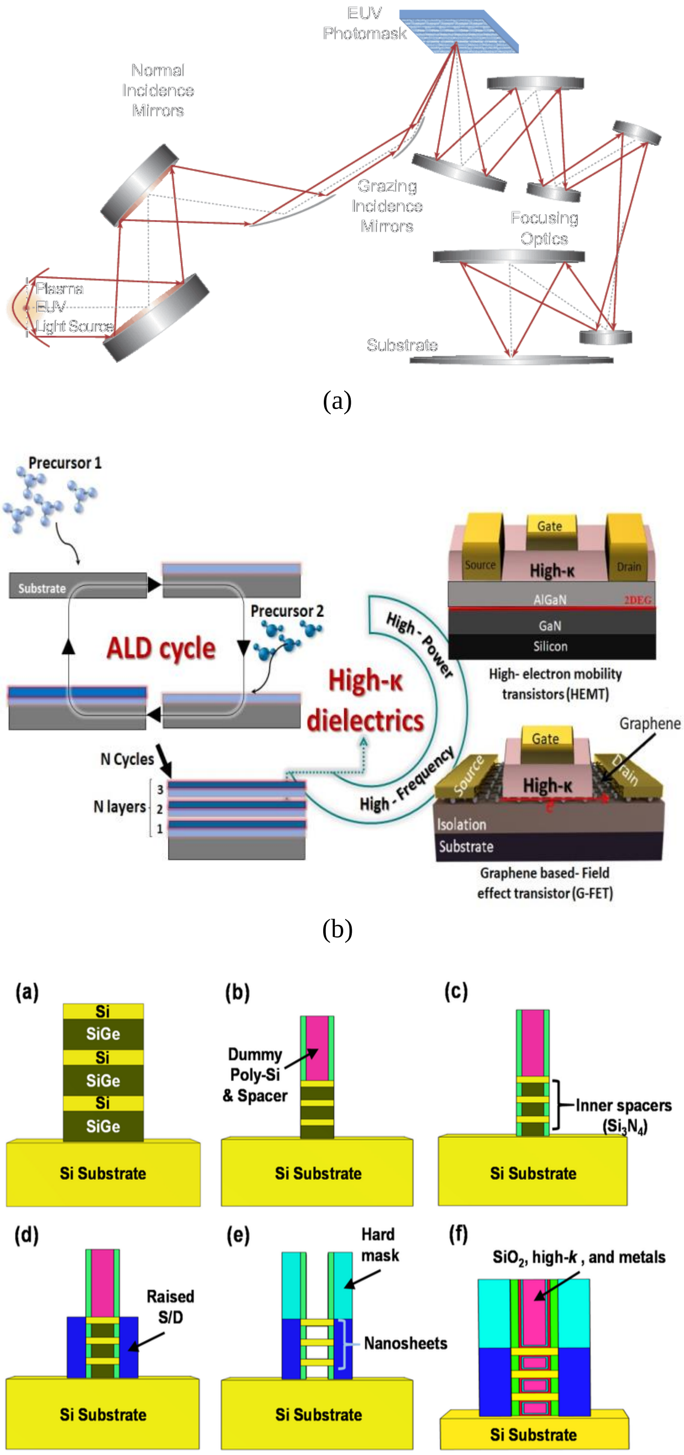

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Figure 4: (a) Key fabrication processes including EUV lithography [17], (b) atomic layer deposition [18], and **(c):** nanosheet epitaxy [19].

6. Integration challenges

Integration challenges extend beyond individual devices to the system level. Contact resistance has emerged as a dominant factor, requiring advanced materials such as cobalt and ruthenium [20]. BEOL scaling faces limitations due to increased resistivity and capacitance [20]. Thermal management is critical in densely packed circuits, particularly in 3D integration, where heat dissipation paths are limited [8,11]. Design rules must also be adapted to ensure manufacturability under advanced lithographic constraints.

7. Case study: FinFET co-optimization

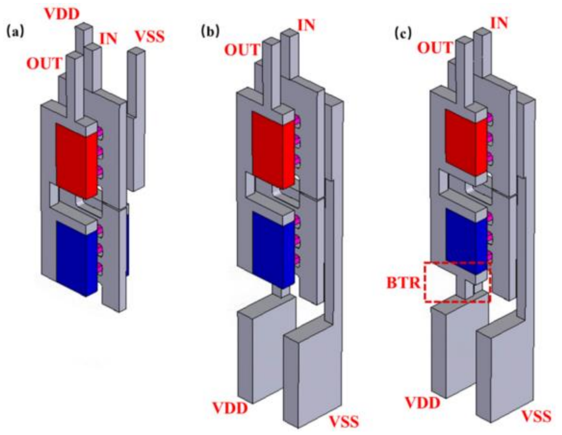
The success of FinFET technology is largely attributed to effective co-optimization. Fin geometry, spacer design, and patterning techniques were optimized alongside layout strategies such as multi-fin quantization and restricted design rules [6]. This holistic approach enabled significant improvements in performance and power efficiency, demonstrating the effectiveness of FICO.

8. GAAFET and nanosheet integration

GAAFET fabrication involves complex processes such as selective epitaxy and channel release etching [5,13]. The integration of high-k/metal gate stacks must ensure conformality around nanosheets. Variability control is critical, as even slight deviations in nanosheet dimensions can significantly impact device performance.

9. CFET and 3D integration

CFET technology introduces new challenges in thermal management, alignment accuracy, and process sequencing. The vertical stacking of transistors increases density but also complicates fabrication and reliability considerations [6,14].



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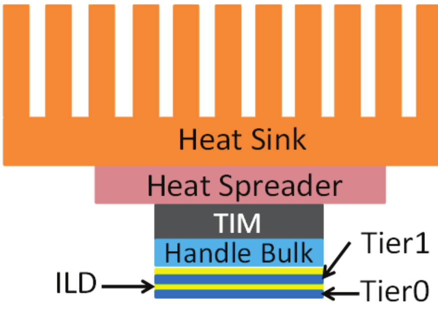

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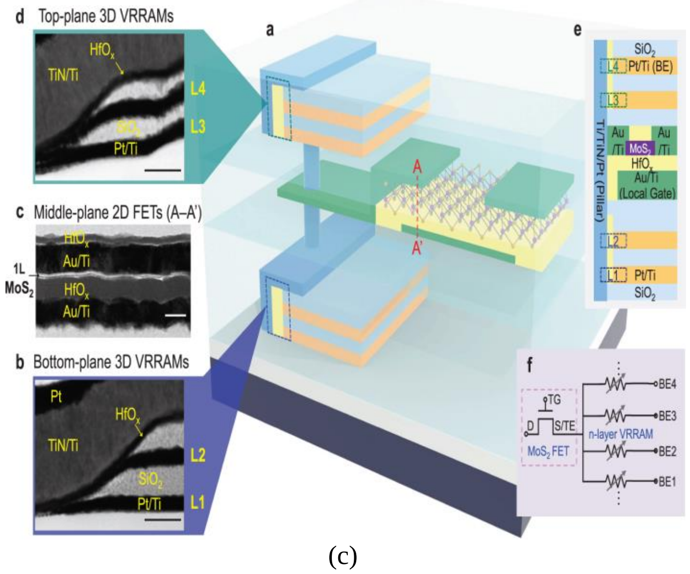

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Figure 5: (a) Illustration of CFET architecture [21] and (b) 3D integration challenges including thermal management [22] and (c) alignment [23].

10. Emerging co-optimization methodologies

Machine learning techniques are increasingly used to optimize fabrication processes by analyzing large datasets from process variations [24]. Virtual fabrication, combining TCAD and EDA tools, enables predictive modeling and reduces development cycles [3,11,25,26].

11. Discussion and future directions

The results and analysis presented in this work highlight a fundamental transition in CMOS technology: performance is no longer device-limited but integration-limited. This shift has profound implications for how future semiconductor technologies must be developed.

Future CMOS scaling will rely heavily on:

- 3D heterogeneous integration
- AI-assisted design and fabrication
- Advanced materials and interconnects

The integration of these technologies will define the next generation of semiconductor innovation [27,28].

12. Conclusion

Fabrication–Integration Co-Optimization is essential for overcoming the limitations of advanced CMOS scaling. By enabling holistic optimization across multiple domains, FICO ensures continued progress in semiconductor technology. In conclusion, the future of semiconductor technology depends not on the ability to fabricate ever-smaller devices, but on the capability to intelligently integrate devices, materials, processes, and systems into a cohesive and optimized framework. FICO stands at the core of this transformation, providing the necessary foundation to sustain innovation beyond the limits of traditional scaling. As the semiconductor industry advances toward increasingly complex and heterogeneous systems, FICO will remain an indispensable strategy for achieving the next generation of high-performance, energy-efficient, and reliable electronic systems.

Authors' contributions

The author reviewed and approved the final version of the manuscript for publication.

Conflicts of interest

The author declares no conflict of interest.

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Data availability

No new data were created.

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